SPECIFICATION
FOR
TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HL MODEL : HG047HD016

☐**Preliminary Specification**

■**Final Specification**

Customer Confirmation column:

Approved by : _____ Dept. : _____ Data : _____

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

Designed by	Checked by	Approved by

Revision History

Version NO.	DATE	Description	Remak
V1.0	2019.02.10	FIRST ISSUE	

CONTENTS

1. GENERAL INFORMATION

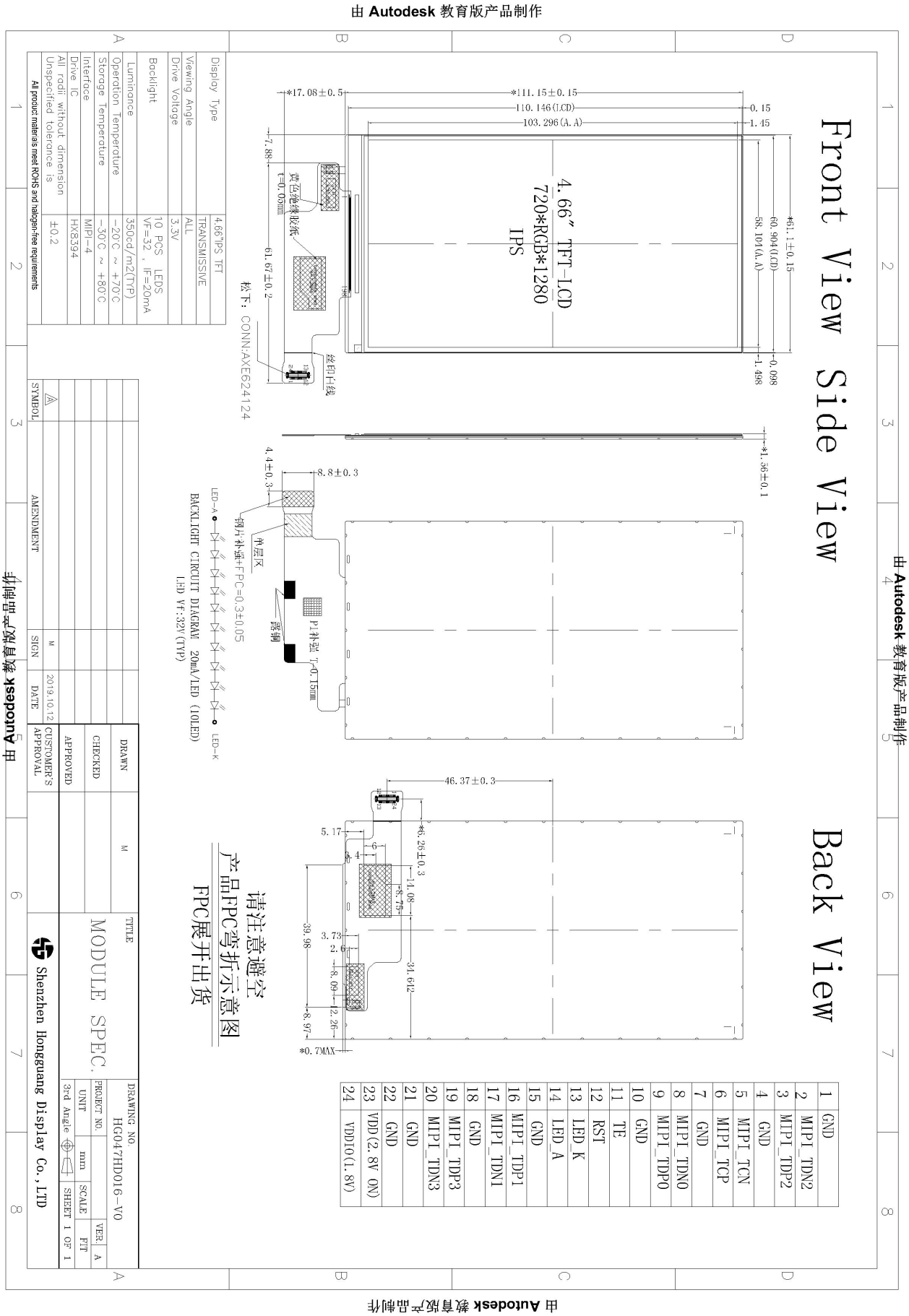
1.1 features

1) Structure: TFT PANNEL+IC+FPC+BL
2) IPS Type LCD 720 dot-segment and 1280 dot-common outputs
3) 16.7M Color can be selected by software
4) White LED back light
5) MIPI interface
6) Operation Temperature : -20~70℃
7) Storage Temperature : -30~80℃
8) CTP cover lens : -/
9) CTP structure : -/
10) LED life time: -/

1.2 General specification

Item of	Contents	Unit
Panel Size	4.7	inch
LCD Type	a-si/TRANSMISSIVE	/
Display mode	Normally Black	/
Pixel arrangement	720*3(RGB)*1280	Dots
Pixel pitch (W*H)	26.9(H)*80.7 (V)	um
Active Area	58.104(H)*103.296(V)	Mm
Module area (W*H*T)	61.1 (H)*111.15(V)*1.56(T)	Mm
Recommended Viewing Direction	ALL	O’ clock
IC	HX8394-A01	/
Interface	4 lane MIPI	/
Luminance for LCM	350	cd/m2
NTSC	70	%
Weight	TBD	g

2. DIAGRAM FOR LCM



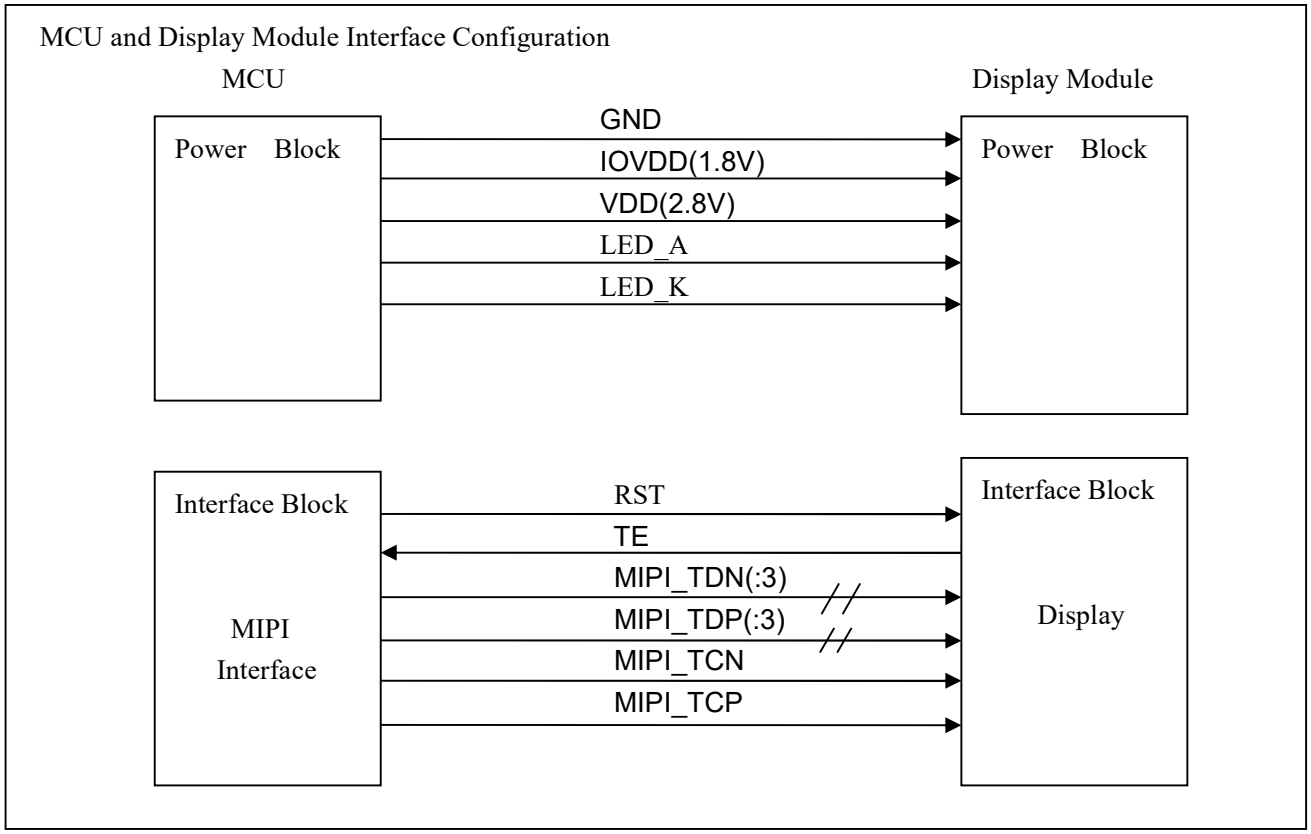
3. I/O CONNECTION & BLOCK DIAGRAM

3.1 I/O connection

LCM Pin	Symbol	I/O	Description
1	**GND**	P	Power Ground
2	**MIPI_TDN2**	I	DSI-D2- differential data signals for MIPI interface
3	**MIPI_TDP2**	I	DSI-D2+ differential data signals for MIPI interface
4	**GND**	P	Power Ground
5	**MIPI_TCN**	I	DSI-CLK- differential clock signals for MIPI interface
6	**MIPI_TCP**	I	DSI-CLK+ differential clock signals for MIPI interface
7	**GND**	P	Power Ground
8	**MIPI_TDN0**	I	DSI-D0- differential data signals for MIPI interface
9	**MIPI_TDP0**	I	DSI-D0+differential data signals for MIPI interface
10	**GND**	P	Power Ground
11	**TE**	I	Tearing effect output pin to synchronize MCU to frame writing
12	**RST**	I	The signal will reset the LCM, Signal is active low.
13	**LED_K**	P	Power supply for LED- cathode
14	**LED_A**	P	Power supply for LED+ anode
15	**GND**	P	Power Ground
16	**MIPI_TDP1**	I	DSI-D1+ differential data signals for MIPI interface
17	**MIPI_TDN1**	I	DSI-D1- differential data signals for MIPI interface
18	**GND**	P	Power Ground
19	**MIPI_TDP3**	I	DSI-D3+ differential data signals for MIPI interface
20	**MIPI_TDN3**	I	DSI-D3- differential data signals for MIPI interface
21	**GND**	P	Power Ground
22	**GND**	P	Power Ground
23	**VDD(2.8V)**	P	A power supply for digital circuits (2.8V)
24	**IOVDD(1.8V)**	P	A power supply for digital circuits and IO pads(1.8V)

I：Input；O：Output；P：Power

3.2 block diagram



4. ABSOLUTE MAXIMUM RATINGS

(GND=AGND=0V)

Parameter of absolute maximum ratings 参数	Symbol 符号	Min 最小值	Max 最大值	Unit 单位
Power voltage supply1	IOVDD(1.8V)	-0.3	3.8	V
Power voltage supply2	VDD(2.8V)	-0.3	3.8	V
Backlight forward current	I_{LED}	-0.001	30	mA(For each led)
Reverse Voltage	V_R	-	5	V
Operating temperature	T_{op}	-20	60	°C
Storage temperature	T_{st}	-30	70	°C
Humidity	RH	-	90%(Max50°C)	RH

5. ELECTRICAL CHARACTERISTICS

5.1 Typical Operation Conditions

Item	Symbol	Values			Unit	Remarks
		Min.	Typ.	Max.		
Power Voltage Supply1	IOVDD(1.8V)	1.65	2.8	3.6	V	
Power Voltage Supply2	VDD(2.8V)	2.8	3.3	3.6	V	
Luminance LCM	Lv	-	350	-	cd/m2	
Backlight Forward Voltage	Vf	-	32	-	V	
LED Forward Current	If	-	20	-	MA	Note

Note:The “LED life time” is defined as the module brightness decrease to 50% of original brightness at I_L=20Ma(for each led). The LED life time could be decreased if operating $I_L$is larger than 20mA

BACKLIGHT CIRCUIT DIAGRAM 20mA/LED (10LED)
LED Vf:32V(TYP)

5.2 DC CHARACTERISTICS

(VDD2=2.5 ~ 3.6V, VDD3=2.5 ~ 3.6V, VDD1=1.65~3.6V, T_A=-40 ~ 85 °C)

Item	Symbol	Unit	Test Condition	Min.	Typ.	Max.	Note
Input high voltage	V_{IH}	V	VDD1= 1.65 ~ 3.6V VDD2= 2.5 ~ 3.6V VDD3= 2.5 ~ 3.6V	0.7 V_{DD1}	-	VDD1	V
Input low voltage	V_{IL}	V		0	-	0.3 V_{DD1}	V
VPP	V_{IH}	V	VPP	7.25V	7.5V	7.75V	V
	V_{IL}	V					
Output high voltage (SDO, CABC_PWM_OUT)	V_{OH1}	V	I_{OH} = -1.0 mA	0.8 V_{DD1}	-	VDD1	V
Output low voltage (SDO, CABC_PWM_OUT)	V_{OL1}	V	VDD1= 1.65 ~ 3.6V I_{OL} = 1.0 mA	0	-	0.2 V_{DD1}	V
Logic High level input current	I_{IH}	uA	VSYNC, HSYNC	-	-	1	uA
			RESX, DCX, CSX, SCL	-	-	1	uA
	I_{IHD}	uA	DB[23:0], SDI, DCX	-	-	1	uA
			DB[23:0]	-	-	1	uA
Logic Low level input current	I_{IL}	uA	VSYNC, HSYNC	-1	-		uA
			RESX, DCX, CSX, SCL	-1	-		uA
	I_{ILD}	uA	DB[23:0], SDI, DCX	-1	-		uA
			DB[23:0]	-1	-		uA
Current consumption standby mode (VDD2/VDD3-VSSD)	$I_{ST(VDD)}$	μA	VDD2/VDD3=2.8V, VDD1=1.8V T_A =25°C	-	10	-	uA
Current consumption standby mode (VDD1– VSSD)	$I_{ST(VDD1)}$	μA		-	10	-	uA

Note: 1. The VPP pin is open on normal mode and in-used while OTP programming condition.

5.3 Reset Timing

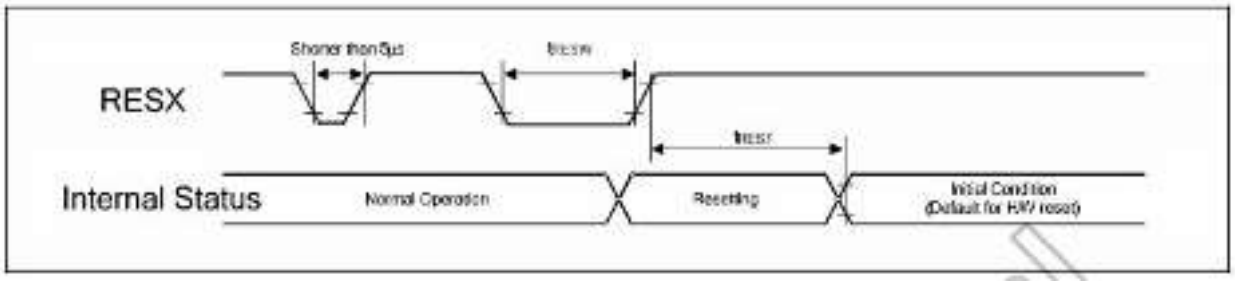


Table 1 Reset Timing

Symbol	Parameter	Related pins	Min.	Typ.	Max.	Note	Unit
t_{RESW}	Reset low pulse width[1]	RESX	10	-	-	-	μs
t_{REST}	Reset complete time[2]	-	5	-	-	When reset is applied during Sleep In mode	ms
		-	120	-	-	When reset is applied during Sleep Out mode	ms

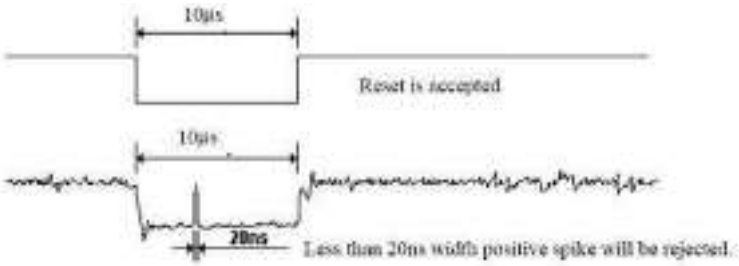
Note: (1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	Action
Shorter than 5 μs	Reset Rejected
Longer than 10 μs	Reset
Between 5 μs and 10 μs	Reset Start

(2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode) and then returns to Default condition for H/W reset.

(3) During Reset Complete Time, ID2 value in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

(4) Spike Rejection also applies during a valid reset pulse as shown below:



(5) When Reset is applied during Sleep In Mode.

(6) When Reset is applied during Sleep Out Mode.

(7) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

5.4 Power Supply On/Off setting sequence

If RESX line is held low (and stable) by the host during power on, then the RESX must be held low for minimum 10μsec after both VDD1, VDD2 and VDD3 have been applied.

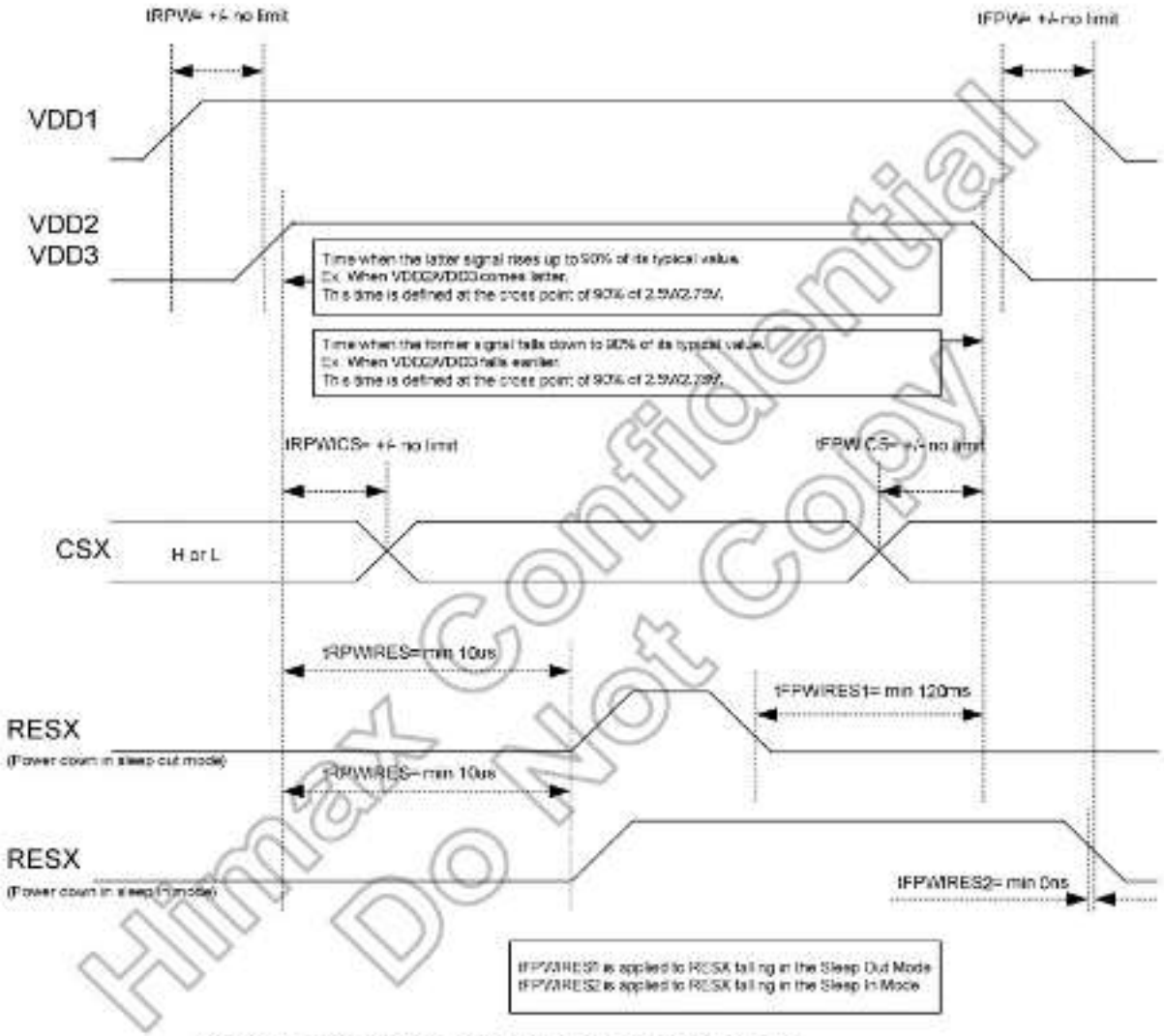
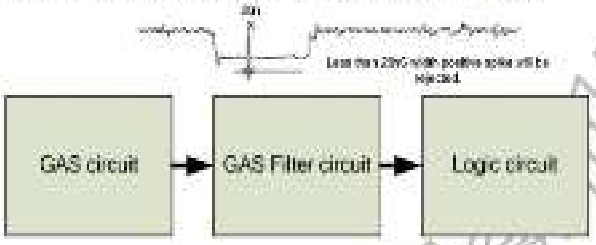


Figure : RESX line is held low by host at power on

Uncontrolled power off

The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damages for the display module or the display module will not cause any damages for the host or lines of the interface. At an uncontrolled power off the display will go blank and there will not be any visible effects within 1 second on the display (blank display) and remains blank until "Power On Sequence" powers it up.

Note: HX8394-A01 is support the noise reject filter (20ns) to reject spike or noise.



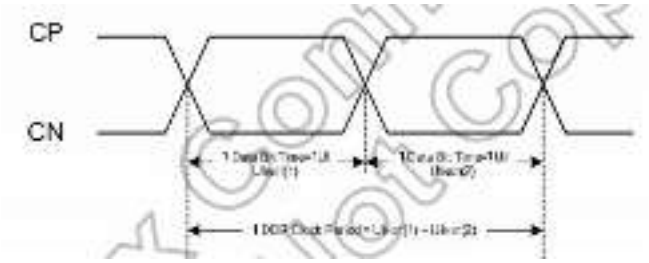
5.5 AC CHARACTERISTICS

5.51 High-Speed Data-Clock Timing

This section specifies the required timings on the high-speed signaling interface independent of the electrical characteristics of the signal. The PHY is a source synchronous interface in the Forward direction.

The Master side of the Link shall send a differential clock signal to the Slave side to be used for data sampling. This signal shall be a DDR (half-rate) clock and shall have one transition per data bit time. All timing relationships required for correct data sampling are defined relative to the clock transitions. Therefore, implementations may use frequency spreading modulation on the clock to reduce EMI.

The DDR clock signal shall maintain a quadrature phase relationship to the data signal. Data shall be sampled on both the rising and falling edges of the Clock signal. The term "rising edge" means "rising edge of the differential signal, i.e. CP – CN, and similarly for "falling edge". Therefore, the period of the Clock signal shall be the sum of two successive instantaneous data bit times. This relationship is shown in Figure .



The same clock source is used to generate the DDR Clock and launch the serial data. Since the Clock and Data signals propagate together over a channel of specified skew, the Clock may be used directly to sample the Data lines in the receiver. Such a system can accommodate large instantaneous variations in UI.

The allowed instantaneous UI variation can cause large, instantaneous data rate variations. Therefore, devices shall either accommodate these instantaneous variations with appropriate FIFO logic outside of the PHY or provide an accurate clock source to the Lane Module to eliminate these instantaneous variations.

The UI_{INST} specifications for the Clock signal are summarized in Table 8.15.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
UI instantaneous	UI_{INST}	-	-	12.5	ns	(1), (2), (3), (4)

Note: (1) This value corresponds to a minimum 80 Mbps data rate.

(2) The minimum UI shall not be violated for any single bit period, i.e., any DDR half cycle within a data burst.

(3) Maximum total bit rate is 1.5Gbps of 3 data lanes 24-bit data format/ 1.12Gbps of 3 data lane 18-bit data format/ 1Gbps of 3 data lane 16-bit data format.

(4) Maximum total bit rate is 2Gbps of 4 data lanes 24-bit data format/ 1.5Gbps of 4 data lane 18-bit data format/ 1.33Gbps of 4 data lane 16-bit data format.

Table 8.15: Reverse HS Data Transmission Timing Parameters

The timing relationship of the DDR Clock differential signal to the Data differential signal is shown in Figure 8.10. Data is launched in a quadrature relationship to the clock such that the Clock signal edge may be used directly by the receiver to sample the received data.

The transmitter shall ensure that a rising edge of the DDR clock is sent during the first payload bit of a transmission burst such that the first payload bit can be sampled by the receiver on the rising clock edge, the second bit can be sampled on the falling edge, and all following bits can be sampled on alternating rising and falling edges.

All timing values are measured with respect to the actual observed crossing of the Clock differential signal. The effects due to variations in this level are included in the clock to data timing budget.

Receiver input offset and threshold effects shall be accounted as part of the receiver setup and hold parameters.

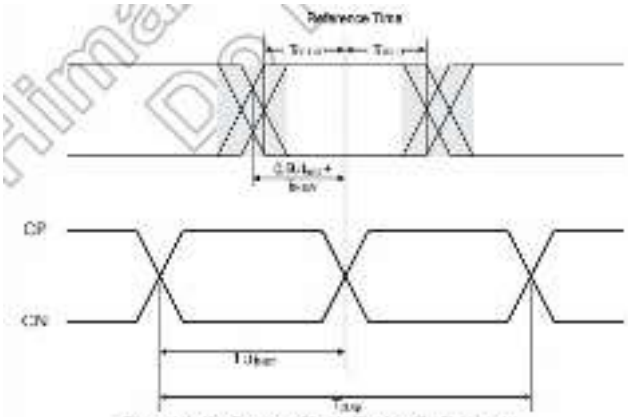


Figure 8.10: Data to Clock Timing Definitions

5.52 High-Speed Data-Clock Timing

The Data-Clock timing specifications are shown in Table 8.16. Implementers shall specify a value UI_{INST},MIN that represents the minimum instantaneous UI possible within a High-Speed data transfer for a given implementation. Parameters in Table 8.16 are specified as a part of this value. The skew specification, $T_{SKEW[TX]}$, is the allowed deviation of the data launch time to the ideal ½UI_{INST} displaced quadrature clock edge. The setup and hold times, $T_{SETUP[RX]}$ and $T_{HOLD[RX]}$, respectively, describe the timing relationships between the data and clock signals. $T_{SETUP[RX]}$ is the minimum time that data shall be present before a rising or falling clock edge and $T_{HOLD[RX]}$ is the minimum time that data shall remain in its current state after a rising or falling clock edge. The timing budget specifications for a receiver shall represent the minimum variations observable at the receiver for which the receiver will operate at the maximum specified acceptable bit error rate.

The intent in the timing budget is to leave 0.4*U_{INST}, i.e. ±0.2*UI_{INST} for degradation contributed by the interconnect.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Data to Clock Setup Time [Receiver]	$T_{SETUP[RX]}$	0.15		-	UI_{INST}	1
Clock to Data Hold Time [Receiver]	$T_{HOLD[RX]}$	0.15	-	-	UI_{INST}	1

Note: (1) Total setup and hold window for receiver of 0.3*UI_{INST}.

Table 8.16: Data to Clock Timing Specifications

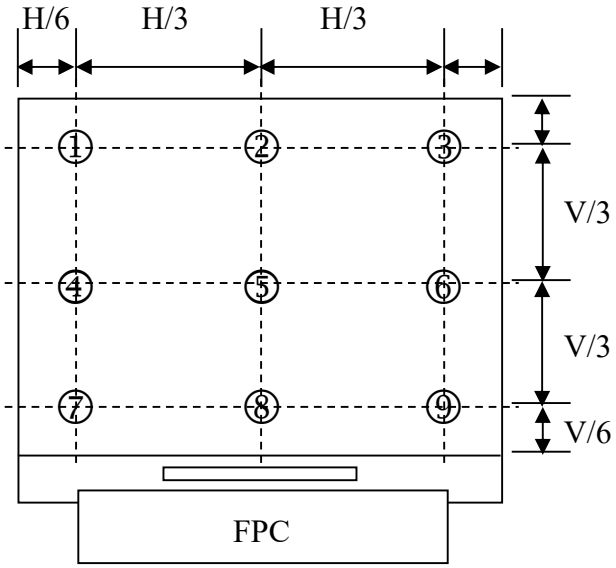
6. ELECTRO-OPTICAL CHARACTERISTICS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio (Center point)		C/R	-	1200	1500	-	-	Note(1)
Luminance uniformity		U_W	θ = 0. Normal viewing angle B/L On Note(1)	80	85	-	%	Note(2)
Response Time		Tr + Tf		-	25	30	ms	Note(3)
Color Chromaticity (CIE 1931)	White	W_X			0.30		参考值	Note(5)
		W_Y			0.32			
	Red	R_X			0.654			
		R_Y			0.319			
	Green	G_X		-0.02	0.259	+0.02		
		G_y			0.574			
	Blue	B_X			0.140			
		B_Y			0.084			
Viewing Angle	Hor.	¢ 3R	C/R≥10		80	-	Deg	Note(4)
		¢ 9L			80	-		
	Ver.	¢ 12U			80	-		
		¢ 6D		-	80	-		

Note1 Definition of Contrast Ratio (CR):

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD on the "White" state}}{\text{Luminance measured when LCD on the "Black" state}}$$

Note2: Definition of Luminance Uniformity: Active area is divided into 9 measuring areas (Shown in below), every measuring point is placed at the center of each measuring area.



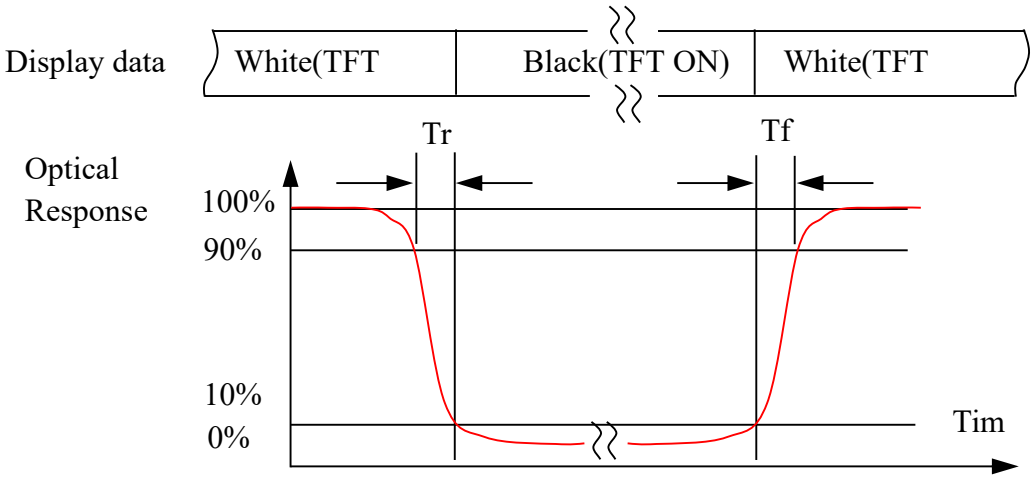
The spot locations for luminance measurement

$$\text{Luminance Uniformity} = \frac{B_{min}}{B_{max}} \times 100\%$$

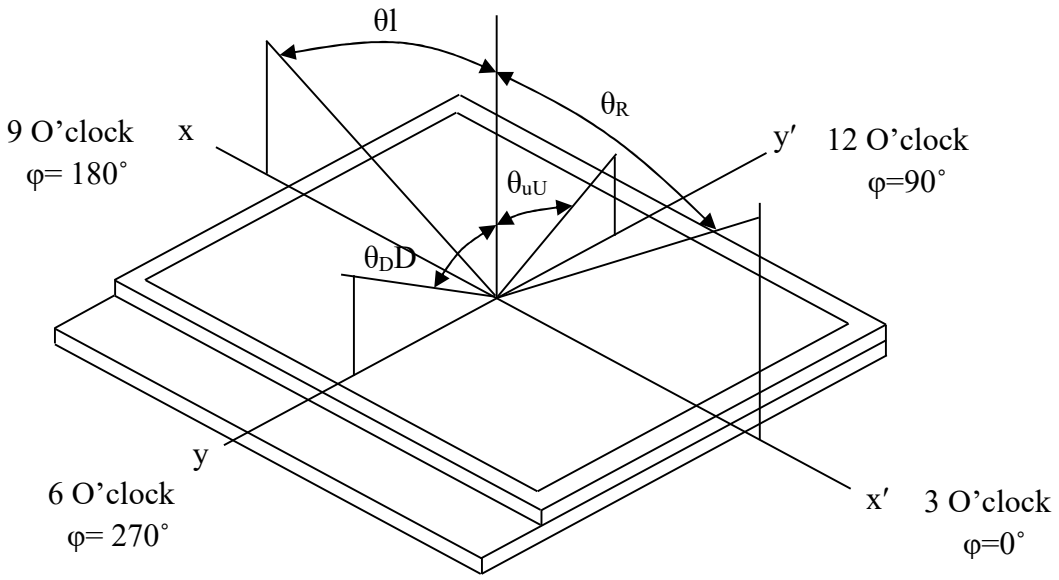
B_{max}: The measured maximum luminance of all measurement position.

B_{min}: The measured minimum luminance of all measurement position.

Note 3:Definition of Response time: Sum of Tr and Tf



Note4.Definition of Viewing Angle: The viewing angle range that the CR≥10



Note 5: Definition of Color Chromaticity (CIE 1931)
Color coordinate of white & red, green, blue at center point.

7. RELIABILITY TEST CONDITIONS

No	Test Item	Test Condition	STANDARD
1	High Temperature Storage	+80°C / 96Hours	1. Functional test is OK. Missing Segment, short, unclear segment, on-display, display abnormally and liquid crystal leak are un-allowed. 2. No low temperature bubbles, end seal loose and fall, frame rainbow.
2	Low Temperature Storage	-30°C / 96Hours	
3	High Temperature Operating	+70°C / 96Hours	
4	Low Temperature Operating	-20°C / 96Hours	
5	Thermal and cold shock	0°C⇆+50°C x 10cycles (30min) (5min) (30min)	
6	Operate at High Temperature and Humidity	60°C x 90%RH / 24H	
7	Vibration Test	Frequency: 10Hz~55Hz~10Hz Amplitude:1.5mm, 2 hours for each direction of X, Y, Z	1. Function test is OK. 2. No glass crack, chipped glass, end seal loose and fall, epoxy frame crack and so on. 3. No structure loose and fall.
8	Dropping test	Drop to the ground from 1m height, 1 corner, 3 edges, 6 surfaces.	
9	ESD test	Contact: ±6KV Air: ±10KV 150PF/330Ω,5Points/panel,5times	The test results shall be subject to the whole machine test.

NOTE:

1. The reliability items will be fully performed in new sample qualification,
2 .The reliability status will be tested as monitor during mass production. Individual reliability test shall be performed by lot , Moreover, the individual reliability item shall be decided according to reliability plan.
3. All samples are inspected after keeping in the room with normal temperature and humidity for 2 hours or above.
4. Vibration test: It is not necessary to test for those products without assembly frame , backlight , PCB and so on.
5. Dropping test : It is necessary for affirming new package.
6. For the high temperature and high humidity test, pure water of over 10 MΩ.cm should be used.
7. Each test item applies for test LCM only once .Then tested LCM cannot be used again in any other test item.
8. The quantity of LCM examination for each test item is 5pcs to 10pcs.

8. INSPECTION STANDARDS

8.1 AQL Sampling inspection standard

使用 GB/T 2828-2003 一般 II 水平,采用正常检查一次抽样方式；具体抽检方式参照《成品检验管理程序》、《抽样管理规范》

缺陷区分	AQL 允收水准
严重缺陷	0 收 1 退
重缺	0.4
轻缺	1.0

8.2 Inspect the condition

8.2.1 在 20—40W 日光灯的照明条件下，样品离检查者眼睛约 30cm 处进行检查。检验方向以垂直线前后左右 45°（以时钟 3 点、6 点、9 点、12 点）

8.2.2 检验者视力需达到标准视力 1.0 以上。

8.2.3 检验者需戴静电手环、两手八个手指套。

8.2.4 外观检验者以目视检查或以菲林对比卡比对。

8.2.5 电性测试使用电测测架,主板,电源线及单片机。

8.2.6 若标准与规格书不符时，以产品发行之规格书特殊检验规格、工程变更为准

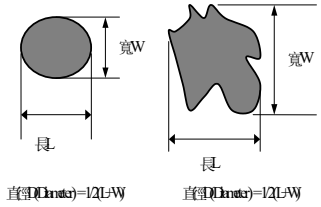
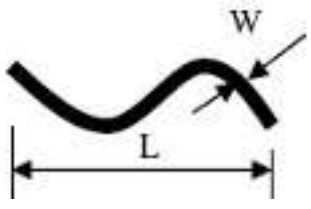
8.2.7 辉色度检测请参照样品,检测方法依照辉色度检验标准。

8.2.8 电测检验环境:照度为 200LUX 以下,外观检验环境: 照度为 600LUX-1000LUX，检验时间：1 秒-3 秒。

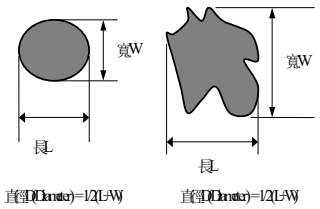
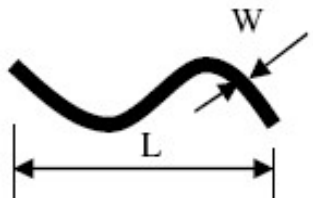
8.2.9 检验工具:电测测架,主板,电源线及单片机,菲林对比卡,游标卡尺,放大镜,实体显微镜(必要时)等等。

8.3 Judgment criterion

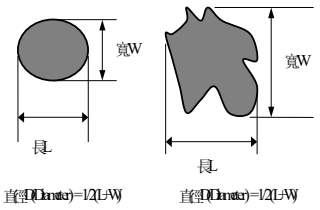
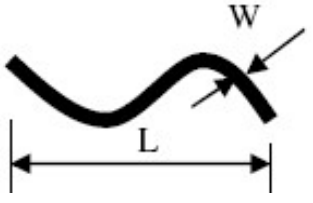
小尺寸点、线判定标准：（6.2 寸以内）

<table>
<tr><td rowspan="6">1</td><td rowspan="6">点状缺陷（磨伤、异物、针孔、凹痕、缺膜、气泡，白点、彩点、脏点）</td><td rowspan="6"> 
</td><td rowspan="5">判定（A/B/C 区）</td><td>D≤0.10,忽略不计,但密集型不允许</td><td rowspan="5">MI</td><td>OK</td></tr>
<tr><td>0.1<D≤0.15，ds≥10</td><td>N≤2</td></tr>
<tr><td>0.15<D≤0.2，ds≥10</td><td>N≤1</td></tr>
<tr><td>LCD 亮点：0.15<D</td><td>N≤1</td></tr>
<tr><td>D>0.2</td><td>NG</td></tr>
<tr><td>判定（D 区）</td><td>同背面丝印油墨区杂质判定标准</td><td></td></tr>
<tr><td colspan="3">注：1）D 区的点状缺陷需在不影响 CTP 功能、客户组装及整机的外观的情况下，判定 OK</td><td>MI</td><td></td></tr>
<tr><td>2</td><td>线状缺陷（磨伤、无感划伤、毛屑、纤维等）</td><td> 
</td><td rowspan="3">判定（A/B/C 区）</td><td>W≤0.03mm，L≤3mmm，ds≥10</td><td rowspan="3">MI</td><td>N≤2</td></tr>
<tr><td>0.03mm<W≤0.05mm，L≤3mm，ds≥10</td><td>N≤1</td></tr>
<tr><td>W>0.05mm 或 L>3mm</td><td>NG</td></tr>
</table>

中尺寸点、线判定标准：（6.2~8 寸以内）

1	点状缺陷（磨伤、异物、针孔、凹痕、缺膜、气泡，白点、彩点、脏点）		判定（A/B/C 区）	*D≤0.10，忽略不计，但密集型不允许*	MI	OK
				0.15<D≤0.25，ds≥10		N≤2
				0.25<D≤3，ds≥10		N≤1
				LCD 亮点：0.2<D		N≤1
				D>0.3		NG
			判定（D 区）	同背面丝印油墨区杂质判定标准		
			注：1）D 区的点状缺陷需在不影响 CTP 功能、客户组装及整机的外观的情况下，判定 OK		MI	
2	线状缺陷（磨伤、无感划伤、毛屑、纤维等）		判定（A/B/C 区）	*W≤0.03mm，L≤3mmm，ds≥10*	MI	N≤2
				0.03mm<W≤0.05mm，L≤3mm，ds≥10		N≤1
				W>0.05mm 或 L>3mm		NG

大尺寸点、线判定标准：（8.1~13.3 寸以内）

1	点状缺陷（磨伤、异物、针孔、凹痕、缺膜、气泡，白点、彩点、脏点）		判定（A/B/C 区）	*D≤0.1，忽略不计，但密集型不允许*	MI	OK
				0.15<D≤0.3，ds≥10		N≤2
				0.3<D≤0.35，ds≥10		N≤1
				LCD 亮点：0.25<D		N≤1
				D>0.35		NG
			判定（D 区）	同背面丝印油墨区杂质判定标准		
			注：1）D 区的点状缺陷需在不影响 CTP 功能、客户组装及整机的外观的情况下，判定 OK		MI	
2	线状缺陷（磨伤、无感划伤、毛屑、纤维等）		判定（A/B/C 区）	*W≤0.05mm，L≤5mmm，ds≥10*	MI	N≤2
				0.05mm<W≤0.07mm，L≤5mm，ds≥10		N≤1
				W>0.07mm 或 L>5mm		NG

9. PACKAGE DRAWING