SPECIFICATION
FOR
TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HG MODEL : HG156FH011

☐**Preliminary Specification**

■**Final Specification**

Customer Confirmation column:

Approved by : _____ Dept. : _____ Data : _____

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1.0 General Descriptions

1.1 Introduction

The HG156FH011 is a color active matrix LCD module incorporation Oxide TFT. Itis composed of a TFT LCD panel, a backlight, a timing controller, voltage reference, common voltage, column driver, and row driver circuit. This TFT LCD has a 15.6-inch diagonally measured active display area with resolution 1,920 horizontal by 1,080 vertical pixel array.

1.2 Features

- 15.6” IPS TFT LCD Panel
- Supported 1,920x1,080 Pixels Resolution
- Compatible With RoHS Standard
- Supported eDP 1.2 Electrical Interface

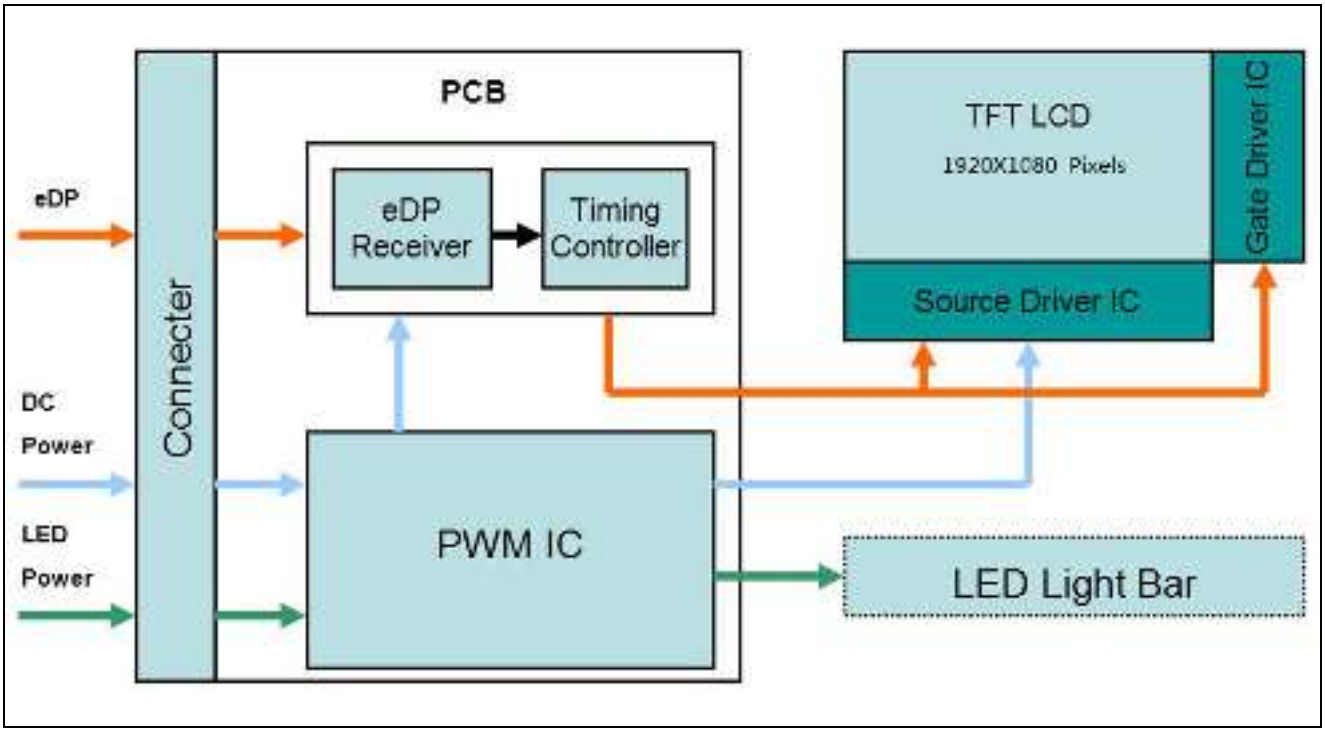
1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	15.6	Inch
Active Area	344.16 (H) x 193.59 (V)	mm
Pixels H x V	1,920 x 1,080	-
Pixel Pitch	0.179 (H) × 0.179 (V)	mm
Pixel Arrangement	R.G.B. Vertical Stripe	-
Display Mode	Normally Black	-
Contrast Ratio	1000	-
White Luminance	1000 (Typ.)	cd/ m^2
Response Time	25	msec
View Angle(L/R/U/D)	89/89/89/89	-
Input Voltage	+3.3 (Logic) / +12V (Backlight)	V
Logic Power Consumption	TBD	Watt
Outline Dimension	360(H) x 222.23(V) x 6.4(D)	mm
Electrical Interface (Logic)	eDP 1.2	-
Support Color	262K	-
Optimum Viewing Direction	ALL	-
Surface Treatment	Anti-glare coating: (3H)	-

1.4 Functional Block Diagram

Figure 1 Shows the functional block diagram of the LCD panel.

Figure 1 Block Diagram



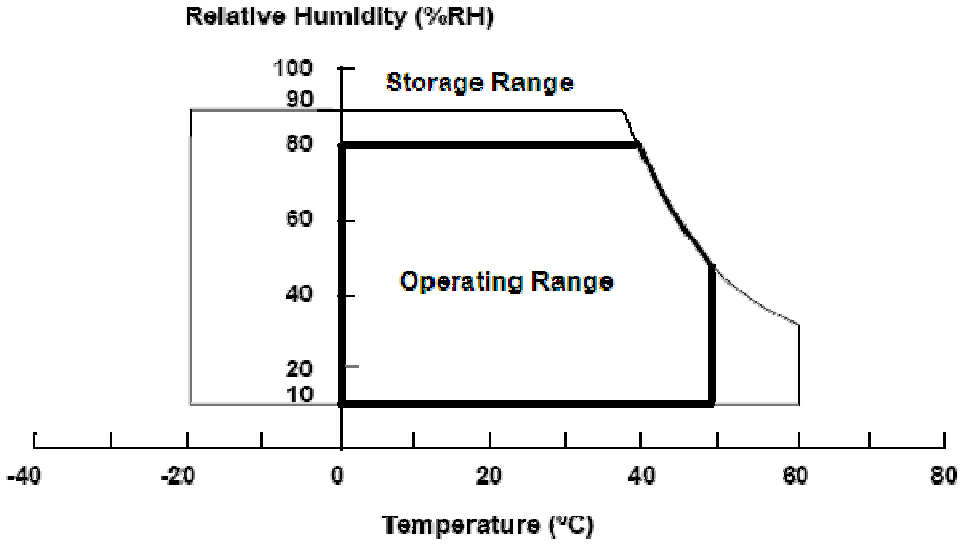
2.0 Absolute Maximum Ratings

Table 1 Absolute Ratings of Enviroment

Item	Symbol	Min.	Max.	Unit	Conditions
Supply Voltage	V_{DD}	-0.3	4.0	V	-
Input Signal	V_S	-0.3	2.4	V	eDP Signals
Operating Temperature	TOP	-25	60	℃	Note
Operating Humidity	HOP	10	80	%RH	Note
Storage Temperature	TST	-30	70	℃	Note
Storage Humidity	HST	10	90	%RH	Note

Note : (A)Maximum Wet-Bulb temperature should be 39℃ and no condensation of water.
(B)When you apply the LCD module for OA system. Please make sure to keep the temperature of LCD module under 60℃.
(C)Storage /Operating temperature & humidity:

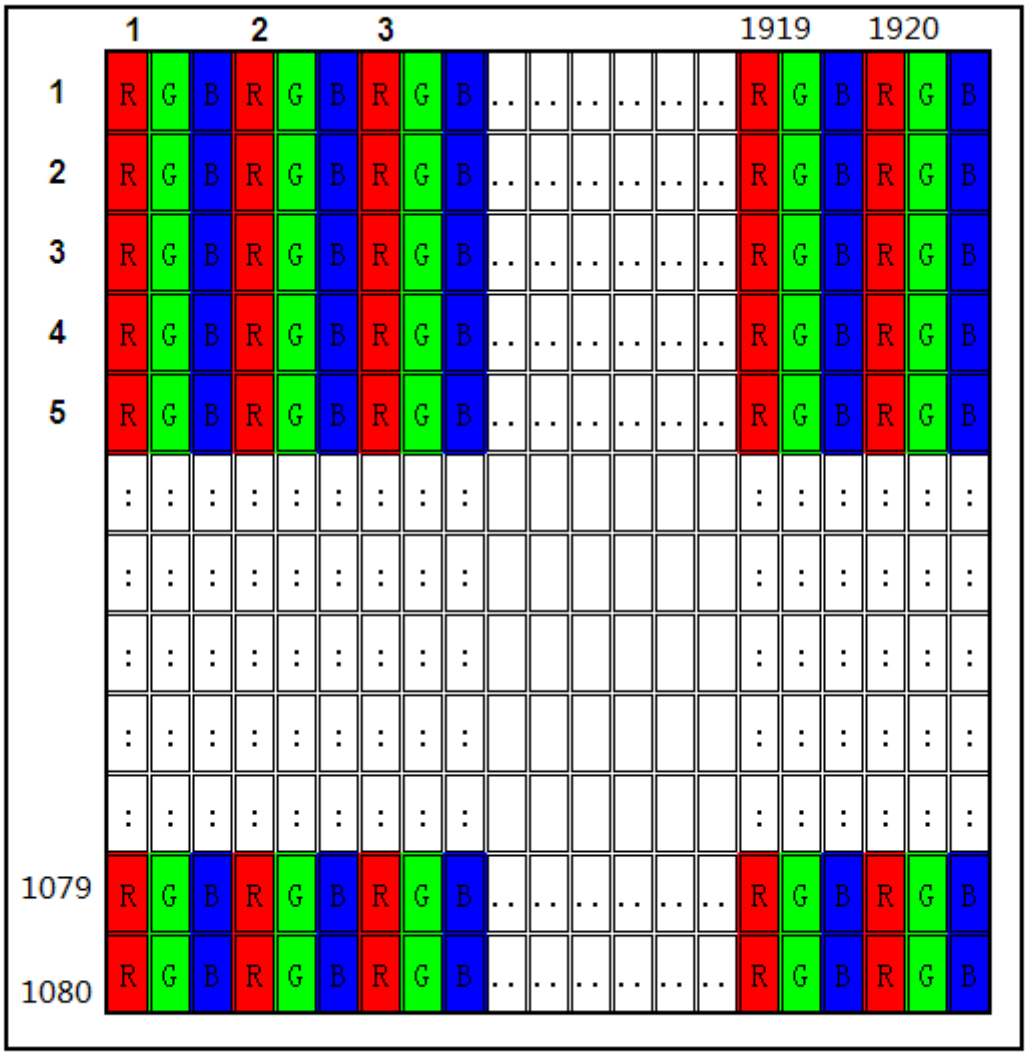
Figure 2 Absolute Ratings of Environment of the LCD Module



3.0 Pixel Format Image

Figure 3 shows the relationship of the input signals and LCD pixels format image.

Figure 3 Pixel Format



4.0 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature) :

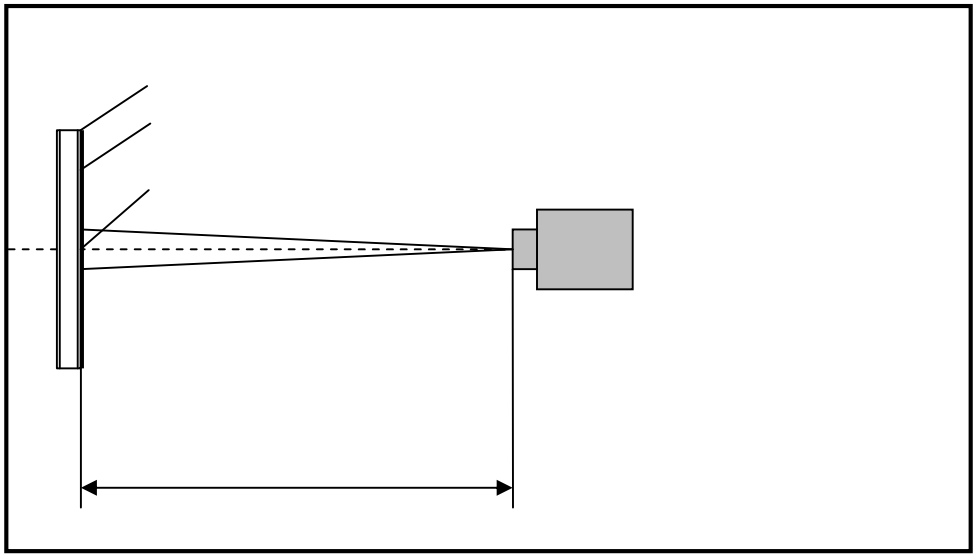
Table 2 Optical Characteristics

Item	Conditions		Specification			
			Min.	Typ.	Max.	Note
Viewing Angle [degrees]	Horizontal CR=10	Left (θ_L)	80	89	-	A, B,C,F,G
		Right (θ_R)	80	89	-	
	Vertical CR=10	Up (ψ_H)	80	89	-	
		Down(ψ_L)	80	89	-	
Contrast Ratio	Center		700	1000	-	A, B,D,F,G
Response Time [ms]	Rising +Falling		-	25	-	A, B,E,F,G
Color /Chromaticity Coodinates (CIE1931)	Red x		Typ-0.03	0.590	Typ+0.03	A,B,F,G
	Red y			0.350		
	Green x			0.330		
	Green y			0.555		
	Blue x			0.153		
	Blue y			0.119		
	White x			0.313		
	White y			0.329		
White Luminance [cd/ m^2]	Y		900	1000	-	A,B
Panel Transmittance [%]	-		-	6.5	-	F,G,H

Note: A. Measurement Setup

The LCD module should be stabilized at 25℃ for 15 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 15 minutes in a windless room.

Figure 4　Measurement Setup



B. The LED input parameter setting as:

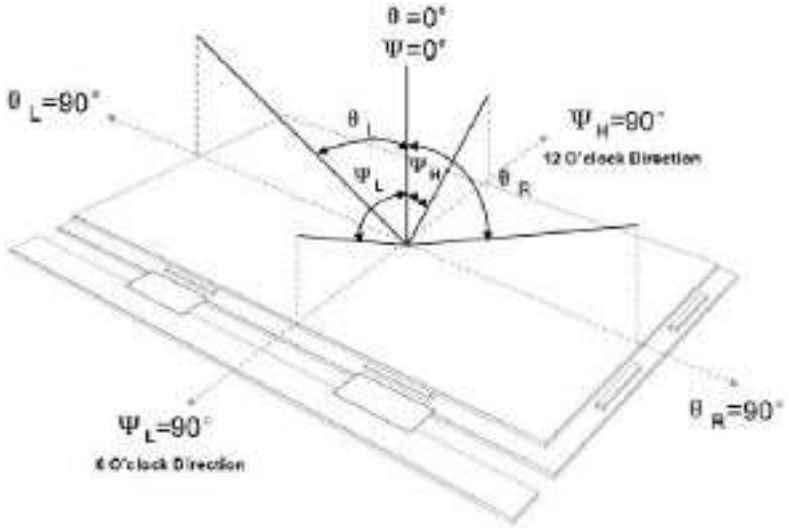
V_LED: 12V (±0.1V)

PWM_LED: duty 100 %

C. Definition of Viewing Angle

Viewing angle is the measurement of contrast ratio ≧10, at the screen center, over a 180° horizontal an 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90°(θ) horizontal left and right and 90° (ψ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.

Figure 5　Definition of Viewing Angle



D. Definition Of Contrast Ratio (CR)

The contrast ratio can be calculated by the following expression

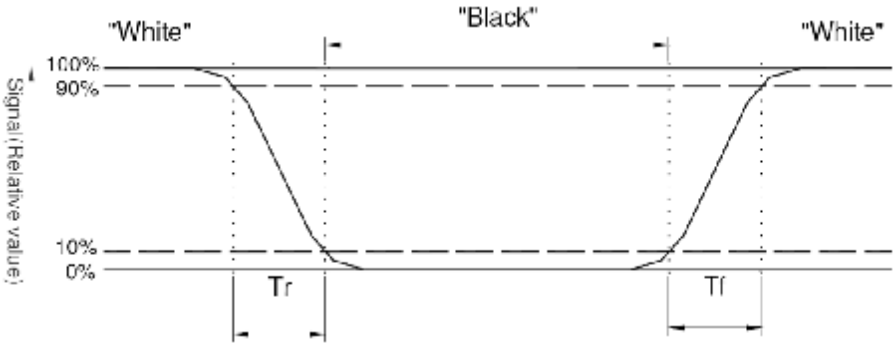
Contrast Ratio (CR) = L63 / L0

L63: Luminance of gray level 63, L0: Luminance of gray level 0

E. Definition Of Response Time (T_r ,T_f)

The output signals of DMS 1140 or equivalent are measured when the input signals are changed from “Black” to “White” (falling time) and from “White” to “Black” (rising time), respectively. The response time interval between the 10% and 90% of amplitudes.

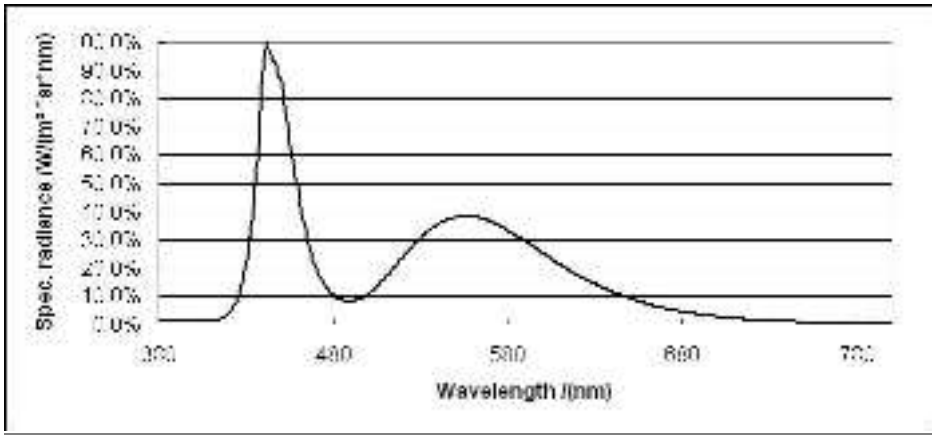
Figure 6 Definition of Response Time



F. Light source is the BLU which is supplied by SWT.

G. SWT Back light Spectrum (Reference)

Figure 7 Back light Spectrum



H. Definition of Center Transmittance(Open-cell is without signal input.)

5.0 Backlight Characteristics(Reference)

Table 3 Backlight Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Units	Condition
VLED	LED input		27	30	33	[V]	Ta=25[deg C]
V_F	LED Forward Voltage		2.9	3.3	3.4	[V]	Ta=25[deg C]
I_F	LED Forward Current			380		[mA]	
P_B/L	B/L Power Consumption		-	-	--	[W]	Ta=25[deg C]
LT	LED Life Time		10000	-	-	Hours	Ta=25[deg C]
VPWM_EN	PWM Signal	High	--	--	--	--	-
		Low	--	--	--	--	
FPWM	Output PWM frequency		--	--	--	--	-
VLED_EN	LED enable	High	--	--	--	--	-
		Low	--	--	--	--	
PWM	PWM Duty ratio		--	--	--	--	-

Note A: Calculator value for LED chip specification.

Note B: The LED life time define as the estimated time to 50% degradation of initial luminous.

6.0 Electrical Characteristics

6.1 Interface Connector

Table 4 Signal Connector Name / Designation

Manufacturer	Starconn
Type / Part Number	300E30-0010RA-G3
Mating Receptacle/Part Number	111B30-1210TA-G3

Table 5 Signal Connector Pin Assignment

Pin	Signal Name	Description	Remarks
1	NC	Not Connect	-
2	GND	Ground	-
3	Lane 1 (N)	Complement Signal Link Lane 1	-
4	Lane 1 (P)	True Signal Line 1	-
5	GND	Ground	-
6	Lane 0 (N)	Complement Signal Link Lane 0	-
7	Lane 0 (P)	True Signal Line 0	-
8	GND	Ground	-
9	AUX_CH(P)	True Signal Auxiliary Ch.	-
10	AUX_CH(N)	Complement Signal Auxiliary Ch.	-
11	GND	Ground	-
12	LCD_VCC	LCD Logic and Driver Power	+3.3V
13	LCD_VCC	LCD Logic and Driver Power	+3.3V
14	NC	Not Connect	-
15	GND	Ground	-
16	GND	Ground	-
17	HPD	HPD Signal Pin	-
18	GND	Ground	-
19	GND	Ground	-
20	GND	Ground	-
21	GND	Ground	-
22	NC	Not Connect	-
23	NC	Not Connect	-
24	NC	Not Connect	-

25	NC	Not Connect	-
26	NC	Not Connect	NC
27	NC	Not Connect	NC
28	NC	Not Connect	NC
29	NC	Not Connect	NC
30	NC	Not Connect	-

Note: All input signals shall be low or Hi-Z state when VDD is off.

6.2 Signal Electrical Characteristics

Input signals shall be low or High-impedance state when VDD is off.

It is recommended to refer the specifications of VESA Display Port Standard V1.2 in detail.

Table 8 Display Port Main Link

Parameter	Description	Min.	Typ.	Max.	Unit
V_{CM}	Differentia Common Mode Voltage	0	-	2.0	V
$V_{Diff\ P-P}$ Level 1	Differential Peak to Peak Voltage Level 1	0.34	0.40	0.46	V
$V_{Diff\ P-P}$ Level 2	Differential Peak to Peak Voltage Level 2	0.51	0.60	0.68	V
$V_{Diff\ P-P}$ Level 3	Differential Peak to Peak Voltage Level 3	0.69	0.80	0.92	V
$V_{Diff\ P-P}$ Level 4	Differential Peak to Peak Voltage Level 4	1.02	1.20	1.38	V

Note: Fallow as VESA display port standard V1.2 at both 1.62 and 2.7Gbps link rates.

Figure 8 Display Port Main Link Signal

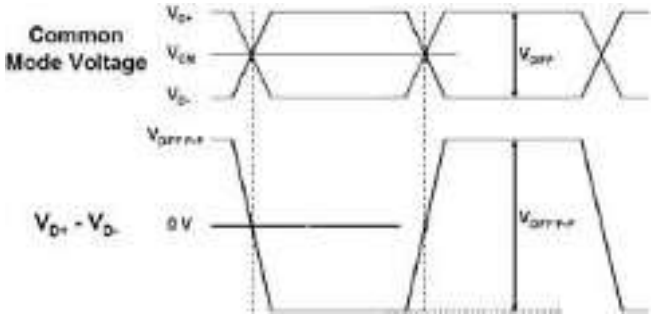


Figure 9 Display Port AUX_CH Signal

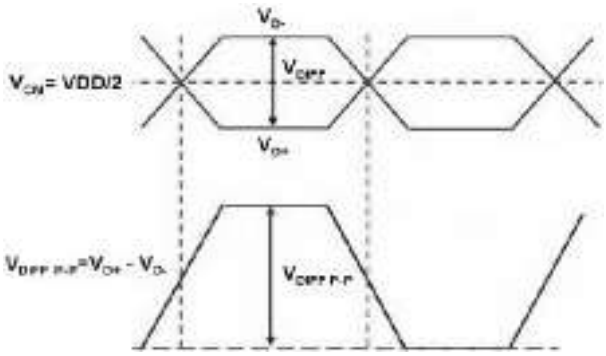


Table 9 Display Port AUX_CH

Parameter	Description	Min.	Typ.	Max.	Unit
V_{CM}	Differentia Common Mode Voltage	0	VDD/2	2	V
$V_{Diff\ P-P}$	Differential Peak to Peak Voltage	0.39	-	1.38	V

Note: Fallow as VESA display port standard V1.2.

Table 10 Display Port V_{HPD}

Parameter	Description	Min.	Typ.	Max.	Unit
V_{HPD}	HPD Voltage	2.25	-	3.60	V

Note: Fallow as VESA display port standard V1.2.

Figure 10 Display Port Interface Power Up/Down Sequence, Normal System Operation

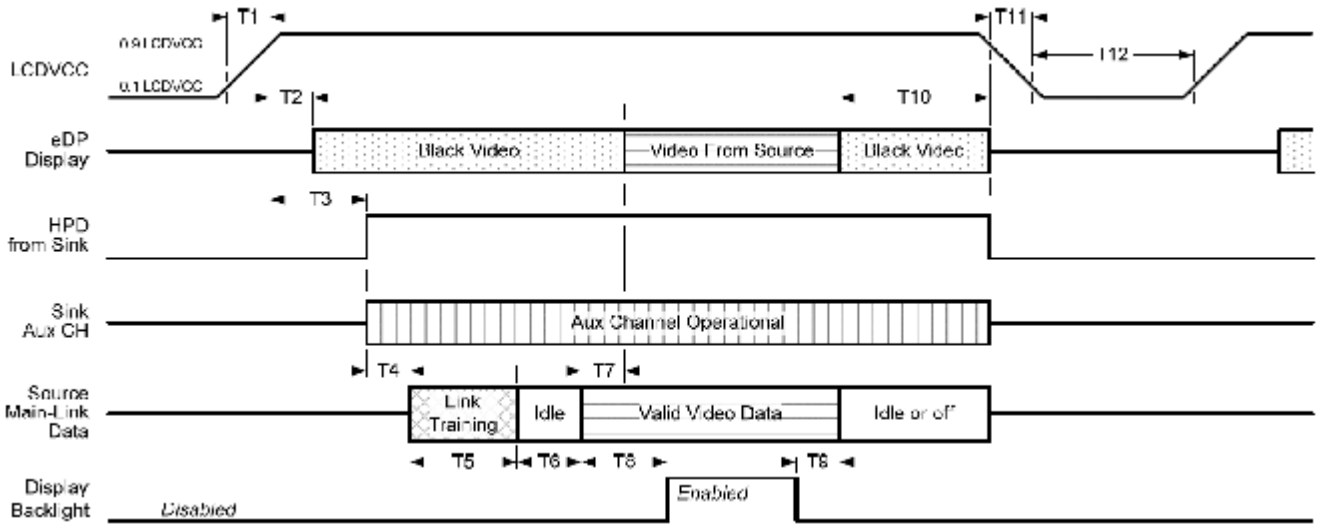


Figure 11 Display Port Interface Power Up/Down Sequence, Aux Channel Transaction Only

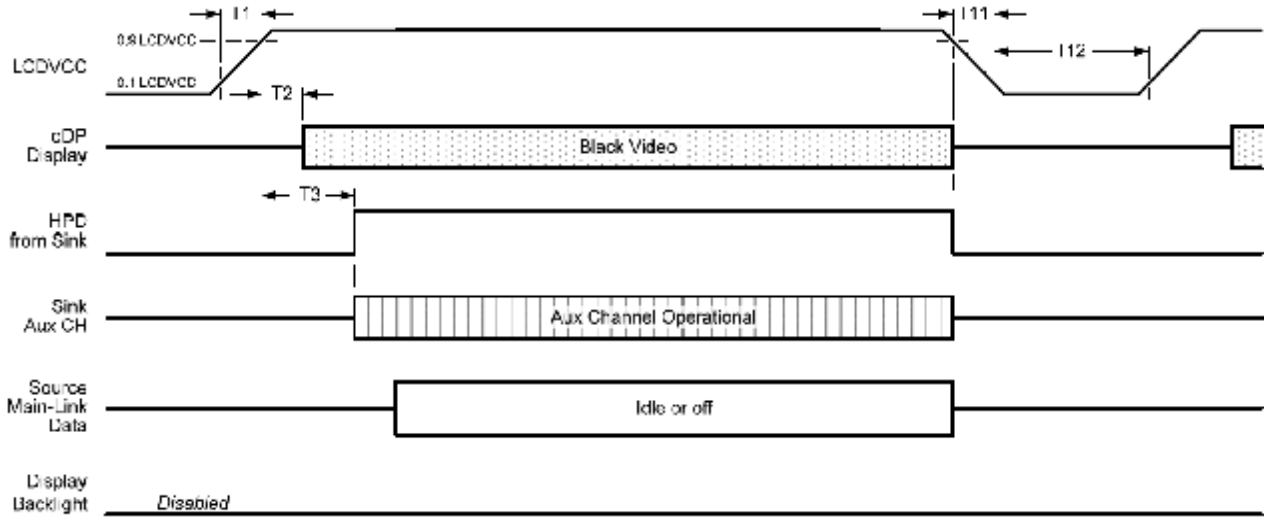


Table 11 eDP Panel Power Sequence Timing Parameters

Timing Parameter	Description	Reqd. By	Limits		Notes
			Min.	Max.	
T1	Power rail rise time, 10% to 90%	Source	0.5ms	10ms	-
T2	Delay from LCD VCC to black video generation	Sink	0ms	200ms	Prevents display noise until valid video data is received from the Source.(see note 1 below)
T3	Delay from LCD VCC to HPD high	Sink	0ms	200ms	Sink Aux Channel must be operational upon HPD high.
T4	Delay from HPD high to link training initialization	Source	-	-	Allows for Source to read Link capability and initialize.
T5	Link training duration	Source	-	-	Dependant on Source link training protocol.
T6	Link idle	Source	-	-	Min accounts for required BS-Idle pattern. Max allows for Source frame synchronization.
T7	Delay from valid video data from Source to video on display	Sink	0ms	50ms	Max allows Sink validate video data and timing.
T8	Delay from valid video from Source to backlight enable	Source	-	-	Source must assure display video is stable.
T9	Delay from backlight disable to end of valid video data	Source	-	-	Source must assure backlight is no longer illuminated.(see note 1 below)
T10	Delay from end of valid video data from Source to power off	Source	0ms	500ms	-

T11	Power rail fall time, 90% to 10%	Source	-	10ms	-
T12	Power off time	Source	500ms	-	-

Note 1: The Sink must include the ability to generate black video autonomously. The Sink must automatically enable black video under the following conditions:
- Upon LCDVCC power-on (within T2 max)
- When the “NoVideoStream_Flag” (VB-ID Bit 3) is received from the Source (at the end of T9)
- When no Main Link data, or invalid video data, is received from the Source. Black video must be displayed within 50ms (max) from the start of either condition. Video data can be deemed invalid based on MSA and timing information, for example.

Note 2: The Sink may implement the ability to disable the black video function, as described in Notes 1, above, for system development and debugging purposes.

Note 3: The Sink must support Aux Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to respond to an Aux Channel transaction with the time specified within T3 max.

7.0 Interface Timings

7.1 Timing Characteristics

Basically, interface timings should match the 1920 x 1080 /60Hz manufacturing guide line timing.

Table 12 Interface Timings

Parameter	Symbol	Unit	Min.	Typ.	Max.
Signal Clock Frequency	f_{dck}	MHz	132	138.5	140
H Total Time	T_{hp}	clocks	2020	2080	2400
H Active Time	HA	clocks		1920	
H Blanking	T_{hfp}	clocks	-	160	-
H Frequency	f_h	kHz	65	66	72
V Total Time	T_{vp}	lines	1090	1111	1200
V Active Time	VA	lines		1080	
V Blanking	T_{vfp}	lines	-	31	-
V Frequency	f_v	Hz	55	60	65

8.0 Power Consumption

Input power specifications are as follows.

The power specification are measured under 25℃ and frame frequency under 60Hz.

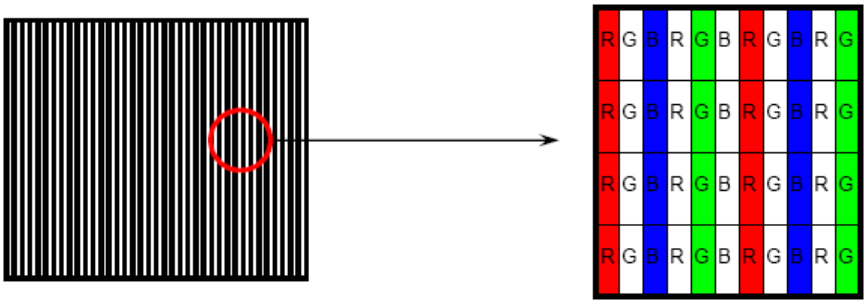
Table 13 Power Consumption

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	V	-
IDD	VDD Current	-	180	260	mA	Note A,
IDD_{MAX}	VDD Current	-	-	260	mA	Note B, C
PDD	VDD Power	-	0.594	0.858	W	Note A, B, C
IRush	Inrush Current	-	-	2	A	Note D, E
VDDrp	Allowable Logic/LCD Drive Ripple Voltage	-	-	100	mV	Vp-p

Note A : IDD_{Black} measurement condition f_{dck}=138.5 MHz, f_v=60Hz, VDD=3.3V, Normal pattern.

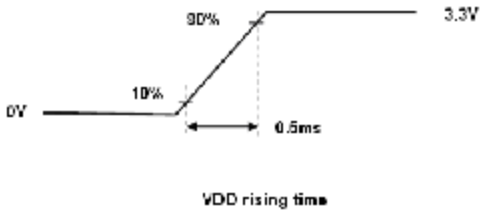
Note B : IDD_{MAX} measurement condition f_{dck}=138.5 MHz, f_v=60Hz, VDD=3.3V, V-Stripe pattern.

Note C : Description of the V-Stripe pattern.



Note D : Measure Condition Figure 12.

Figure 12 VDD Rising Time



Note E : When the IRush Measure Condition at VDD rising time=1.5ms, the value of IRush(Typ.)= 1A.

9.0 Power ON/OFF Sequence

VDD power on/off sequence is as follows. Interface signals are also shown in the chart.

Signals from any system shall be Hi-Z state or low level when VDD is off.

Figure 13 Power Sequence

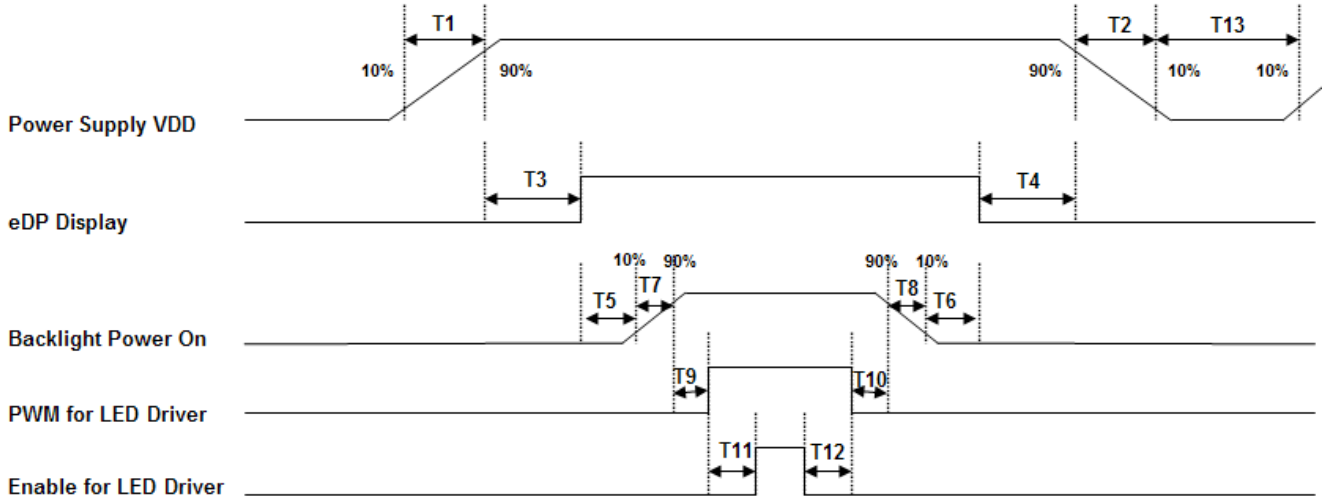
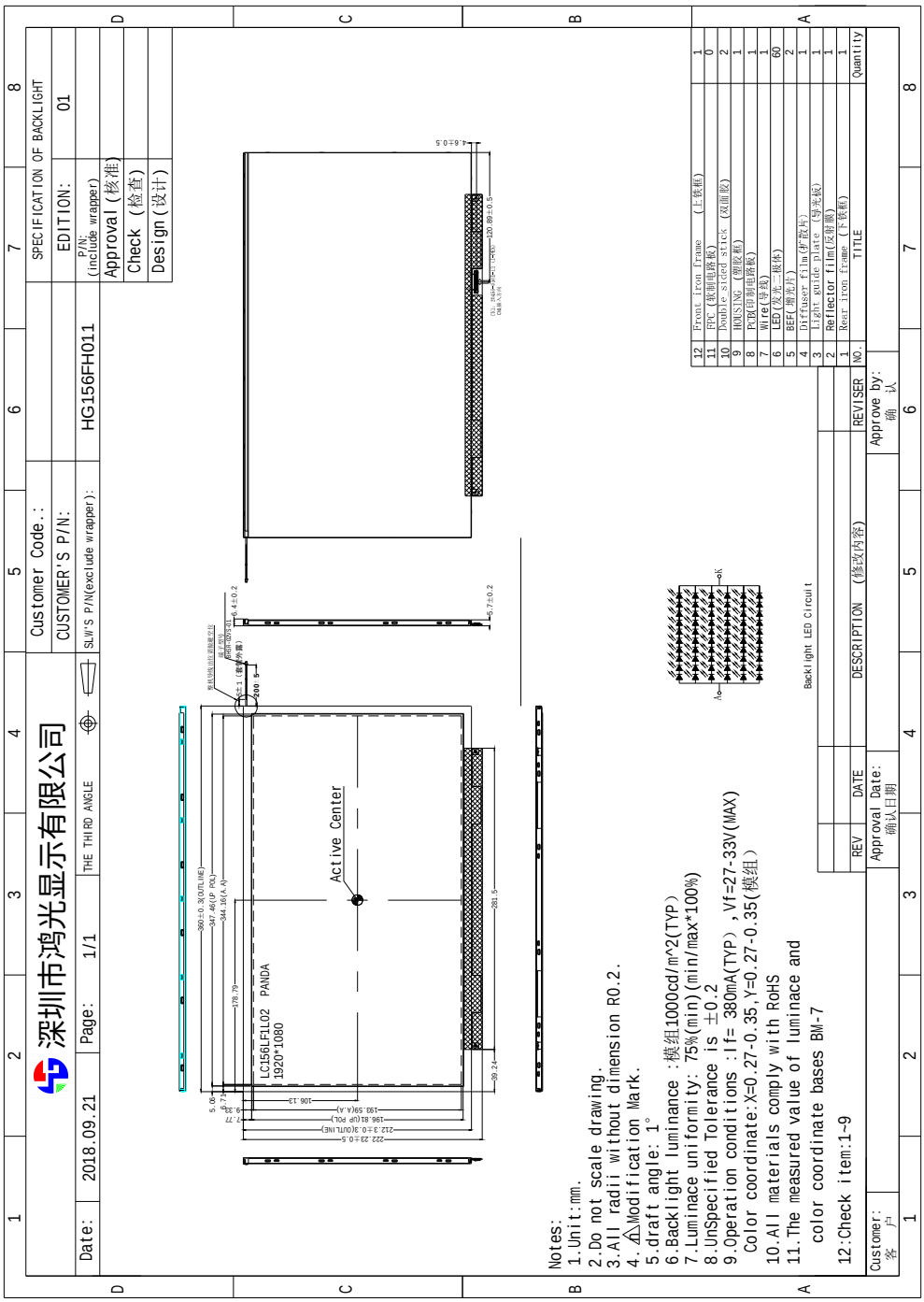


Table 15 Power Sequencing Requirements

Parameter	Unit	Min.	Max.
T1	ms	0.5	10
T2	ms	0	10
T3	ms	0	200
T4	ms	0	50
T5	ms	300	-
T6	ms	200	-
T7	ms	0.5	10
T8	ms	0	10
T9	ms	10	-
T10	ms	10	-
T11	ms	10	-
T12	ms	0	-
T13	ms	500	-

10.0 Mechanical Characteristics

Figure 14 Reference Outline Drawing



11.0 Package Specification

TBD

12.0 General Precaution

12.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life-threatening or otherwise catastrophic.

12.2 Handling Precaution

(1) Please mount LCD panel by using mounting holes arranged in four corners tightly.

(2) Do not disassemble or modify the panel. It may damage sensitive parts inside LCD panel, and may cause scratches or dust on the display. SWT does not warrant the panel, if customers disassemble or modify the panel.

(3) If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid Crystal, and do not contact liquid crystal with skin. If liquid crystal contacts mouth or eyes, rinse out with water immediately. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and Rinse thoroughly with water.

(4) Disconnect power supply before handling LCD panel.

(5) Refrain from strong mechanical shock and /or any force to the panel.

(6) Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature; etc otherwise LCD panel may be damaged. It's recommended employing protection circuit for power supply.

(7) Do not touch, push or rub the polarizer with anything harder than HB pencil lead. Use fingerstalls of soft gloves in order to keep clean display quality, when Persons handle the LCD panel for incoming inspection or assembly.

(8) When the surface is dusty, please wipe gently with absorbent cotton or other soft Material. When cleaning the adhesives, please use absorbent cotton wetted with a little Petroleum benzene or other adequate solvent.

(9) Wipe off saliva or water drops as soon as possible. If saliva or water drops Contact with polarizer for a long time, they may causes deformation or color Fading.

(10) Protection film must remove very slowly from the surface of LCD panel to prevent from electrostatic occurrence.

(11) Because LCD panel uses CMOS-IC on circuit board and TFT-LCD panel, it is Very weak to electrostatic discharge, Please be careful with electrostatic Discharge .Persons who handle the panel should be grounded through adequate methods.

(12) Do not adjust the variable resistor located on the panel.

12.3 Storage Precaution

(1) Please do not leave LCD panel in the environment of high humidity and high temperature for a long time.

(2) The panel shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

(3) The panel should be stored in a dark place. It is prohibited to apply sunlight or fluorescent light in storage.

12.4 Operation Precaution

(1) Do not connect or disconnect the panel in the "Power On" condition.

(2) Power supply should always be turned on/off by 9.0 "Power ON/OFF Sequence".

(3) Panel has high frequency circuits. Sufficient suppression to the electromagnetic interference

should be done by system manufacturers. Grounding and shielding methods may be important to minimize the interference.

(4) After installation of the TFT Panel into an enclosure, do not twist nor bend the TFT Panel even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Panel from outside. Otherwise the TFT Panel may be damaged.

12.5 Others

(1) Ultra-violet ray filter is necessary for outdoor operation.

(2) Avoid condensation of water which may result in improper operation or disconnection of electrode.

(3) If the panel keeps displaying the same pattern for a long period of time, the image may be "sticked" to the screen.

(4) This panel has its circuitry PCB's on the rear side and should be handled carefully in order not to be stressed.

12.6 Disposal

When disposing LCD panel, obey the local environmental regulations.