SPECIFICATION

FOR

TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HL MODEL : HG007WS003

□**Preliminary Specification**

■**Final Specification**

Customer Confirmation column:

Approved by :_____Dept. :_____Data :_____

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

Designed by	Checked by	Approved by

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	■ INITIAL RELEASE	2021. 10. 20	
A01	■ Add the package	2022. 04. 02	

CONTENTS

1. WARRANTY

Supplier warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). Supplier is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored in the original packages at 25°C±5°C, 55%±10%RH or used as the conditions specified in the specifications.

Nevertheless, Supplier is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

2. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel resolution : 64x48
- Driver IC : SSD1315
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.26 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8-bit 6800/8080-series parallel interface, 4 wire Serial Peripheral Interface, I2C Interface
- Wide range of operating temperature : -40 to 70°C
- Anti-glare polarizer.

3. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	64(W) x 48(H)	dot
2	Dot Size	0.185 (W) x 0.185(H)	mm^2
3	Dot Pitch	0.210(W) x 0.210 (H)	mm^2
4	Aperture Rate	78	%
5	Active Area	13.42 (W) x 10.06 (H)	mm^2
6	Panel Size	18.46(W) x 18.10(H)	mm^2
7*	Panel Thickness	1.05	mm
8	Module Size	18.46 (W) x27.9(H) x 1.26 (T)	mm^3
9	Diagonal A/A size	0.66	inch
10	Module Weight	0.84±10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

4. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	4	V	Ta = 25°C	IC maximum rating
Supply Voltage (V_{BAT})	-0.3	5	V	Ta = 25°C	IC maximum rating
Supply Voltage (Vcc)	6	15	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		-
Storage Temp	-40	80	°C		Note (2)

Note:

(1) Maximum ratings are those values beyond which damages to the OLED module may occur. The OLED functional operation should be restricted to the limits in the section 5. Electrical Characteristics tables.

(2) The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

5. ELECTRICAL CHARACTERISTICS

5.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{DD}	Logic Supply Voltage	Ta = 25°C	1.65	3.3	3.5	V
V_{BAT}	Charge Pump Regulator Supply Voltage	Ta = 25°C	3.5	3.6	4.2	V
V_{CC}	Operating Voltage (for OLED panel)	Ta = 25°C	7	7.5	-	V
V_{OH}	High Logic Output Level	I_{OUT} = 100uA, 3.3MHz	0.9* V_{DD}	-	-	V
V_{OL}	Low Logic Output Level	I_{OUT} = 100uA, 3.3MHz	-	-	0.1*V_{DD}	V
V_{IH}	High Logic Input Level	-	0.8* V_{DD}	-	-	V
V_{IL}	Low Logic Input Level	-	-	-	0.2*V_{DD}	V

5.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current consumption (IBAT) (Charge Pump)	-	14	17	mA	All pixels on (1)
IDD sleep mode current	-	-	10	uA	Sleep mode Current (2)
ICC sleep mode current	-	-	10	uA	Sleep mode Current (2)
Pixel Luminance(Charge Pump)	90	110		cd/m^2	Display Average
CIEx (White)	0.24	0.28	0.32		CIE1931
CIEy (White)	0.28	0.32	0.36		CIE1931
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition : (Charge Pump)

- VBAT = 3.6V
- Contrast setting : 0X7D
- Charge Pump Setting:0x14
- Frame rate : 105Hz
- Duty setting : 1/48

(2) Sleep mode condition :

When send 0xae command OLED display off and memory data will be maintained.

(3) Wake up condition :

When send 0xaf command OLED will be turned on.

6. LIFETIME SPECIFICATION

ITEM	MIN	UNIT	Condition	Remark
Life Time	20,000	Hrs	110 cd/m², alternating checkerboard	Note (1)

Note:

(A) Under VBAT = 3.6V (Charge Pump), Ta = 25°C, 50% RH.

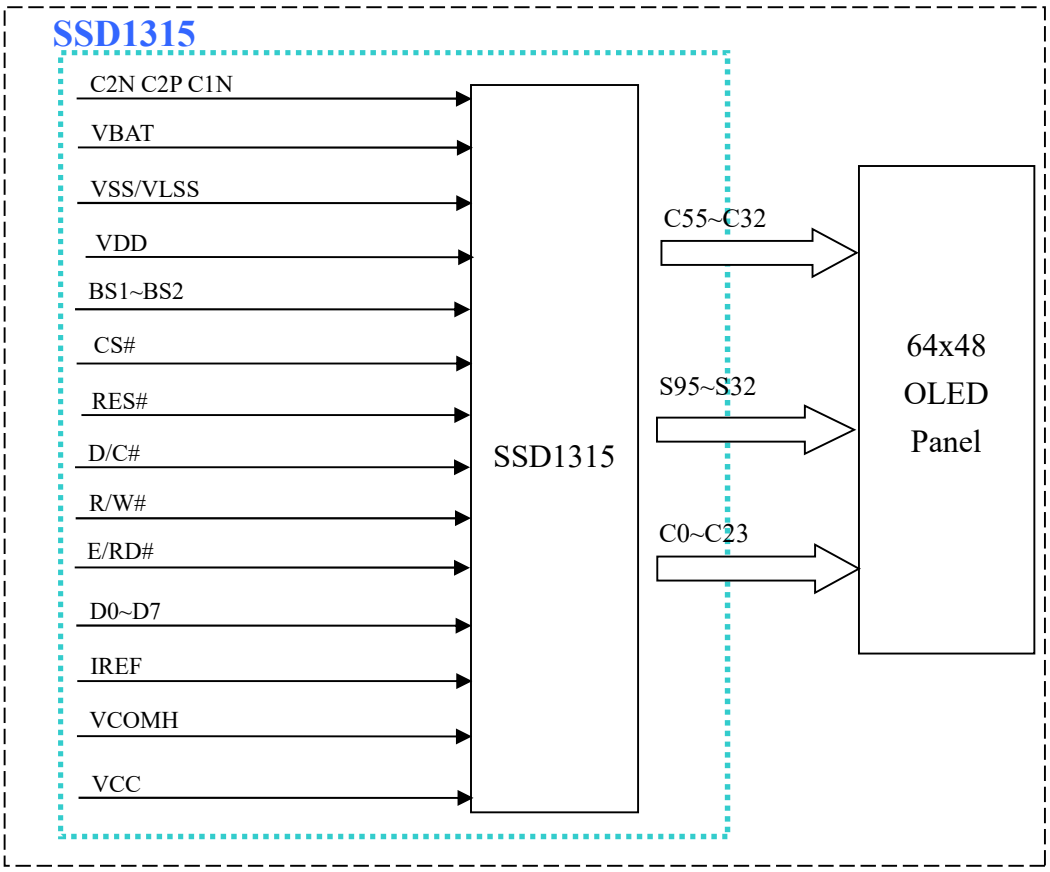
(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 110cd/m² : (Charge Pump)

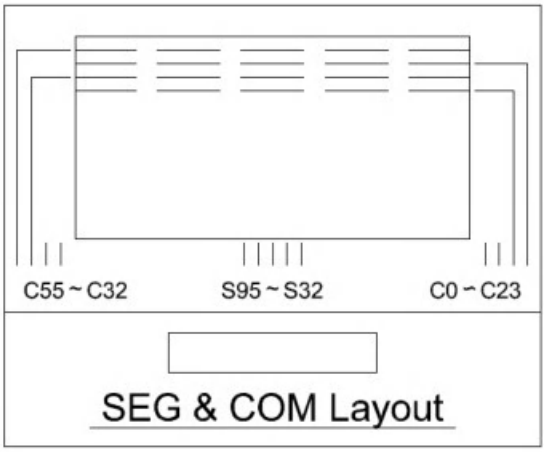
- Contrast setting : 0x7D
- Charge Pump Setting:0x14
- Frame rate : 105Hz
- Duty setting : 1/48

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

<table>
<tr><th>No.</th><th>Symbol</th><th>Function</th></tr>
<tr><td>1</td><td>NC.
(GND)</td><td>Reserved Pin (Supporting Pin)
The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.</td></tr>
<tr><td>2</td><td>C2N</td><td rowspan="4">Positive Terminal of the Flying Inverting Capacitor Negative Terminal of the Flying Boost Capacitor The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.</td></tr>
<tr><td>3</td><td>C2P</td></tr>
<tr><td>4</td><td>C1P</td></tr>
<tr><td>5</td><td>C1N</td></tr>
<tr><td>6</td><td>VBAT</td><td>Power Supply for DC/DC Converter Circuit
This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to VDD when the converter is not used.</td></tr>
<tr><td>7</td><td>VSS</td><td>Ground of Logic Circuit
This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>8</td><td>VDD</td><td>Power Supply for Logic
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>9</td><td>BS1</td><td rowspan="2">MCU bus interface selection pin.
<table>
<tr><td>Interface</td><td>SPI 4</td><td>IIC</td><td>8bits 8080</td><td>8bits 6800</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>0</td><td>0</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>10</td><td>BS2</td></tr>
<tr><td>11</td><td>CS#</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>12</td><td>RES#</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>13</td><td>D/C#</td><td>Data/Command Control
This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data.
When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
When the pin is pulled high and serial interface mode is selected, the data at SDIN is treated as data. When it is pulled low, the data at SDIN will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection.</td></tr>
<tr><td>14</td><td>R/W#</td><td>Read/Write Select or Write
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection</td></tr>
</table>

		input. Pull this pin to“High” for read mode and pull it to “Low” for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
15	E/RD#	*Read/Write Enable or Read* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.
16~23	D0~D7	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK. When I2Cmode is selected, D2 & D1 should be tired together and serve as SDAout & SDAin in application and D0 is the serial clock input SCL.
24	IREF	*Current Reference for Brightness Adjustment* This pin is segment current reference pin. A resistor should be connected between this pin and VSS.
25	VCOMH	*Voltage Output High Level for COM Signal* This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.
26	VCC	*Power Supply for OEL Panel* This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and VSS when the converter is used. It must be connected to external source when the converter is not used.
27	VLSS	*Ground of Analog Circuit* This is an analog ground pin. It should be connected to VSS externally.
28	NC (GND)	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins. These pins must be connected to external ground.

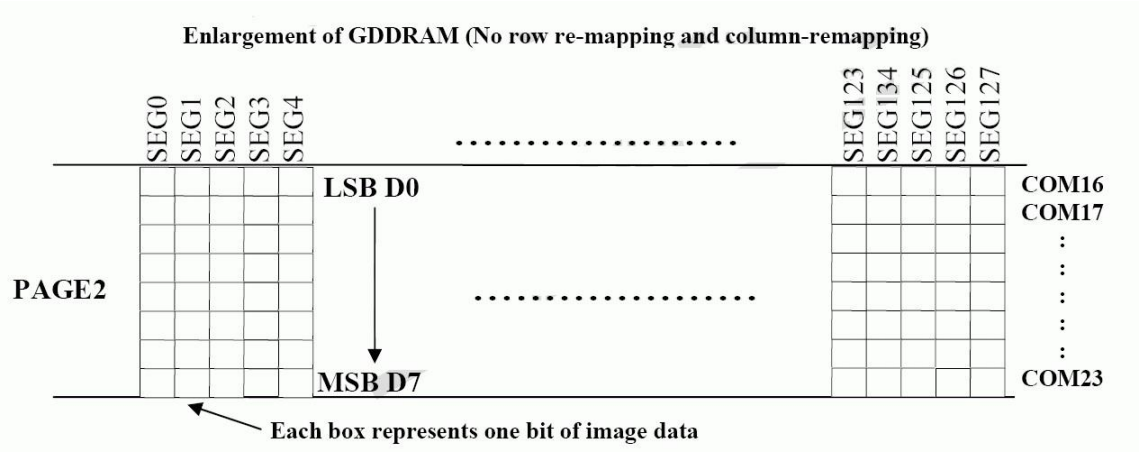
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 128 x 64 bits and the RAM is divided into eight pages, from PAGE0 to PAGE7, which are used for monochrome 128x64 dot matrix display, as shown in below figures.

GDDRAM pages structure

		Row re-mapping
PAGE0 (COM0-COM7)	Page 0	PAGE0 (COM 63-COM56)
PAGE1 (COM8-COM15)	Page 1	PAGE1 (COM 55-COM48)
PAGE2 (COM16-COM23)	Page 2	PAGE2 (COM47-COM40)
PAGE3 (COM24-COM31)	Page 3	PAGE3 (COM39-COM32)
PAGE4 (COM32-COM39)	Page 4	PAGE4 (COM31-COM24)
PAGE5 (COM40-COM47)	Page 5	PAGE5 (COM23-COM16)
PAGE6 (COM48–COM55)	Page 6	PAGE6 (COM15-COM8)
PAGE7 (COM56-COM63)	Page 7	PAGE7 (COM 7-COM0)
	SEG0 ----------SEG127	
Column re-mapping	SEG127 ----------SEG0	

When one data byte is written into GDDRAM, all the rows image data of the same page of the current column are filled (i.e. the whole column (8 bits) pointed by the column address pointer is filled.). Data bit D0 is written into the top row, while data bit D7 is written into bottom row as shown in below figures.



For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software.

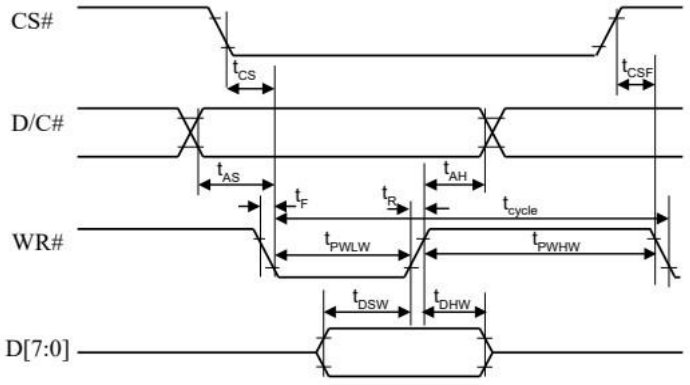
For vertical shifting of the display, an internal register storing the display start line can be set to control the portion of the RAM data to be mapped to the display (command D3h).

7.5 INTERFACE TIMING CHART

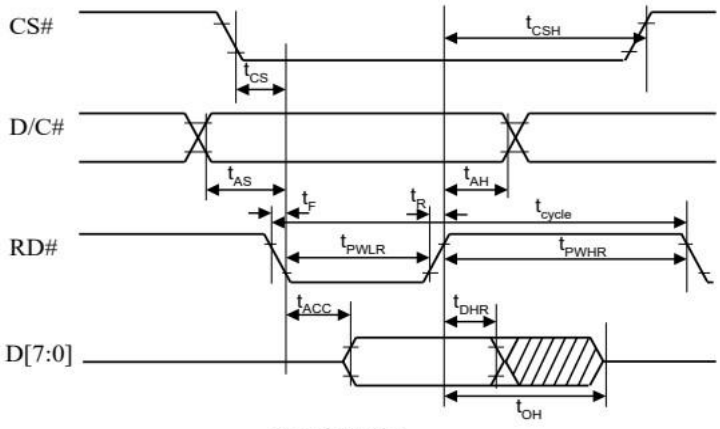
7.5.1 8080 8bits Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V ~3.5V, T_A = 25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	20	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	180	ns
t_{PWLR}	Read Low Time	180	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns



Write Cycle

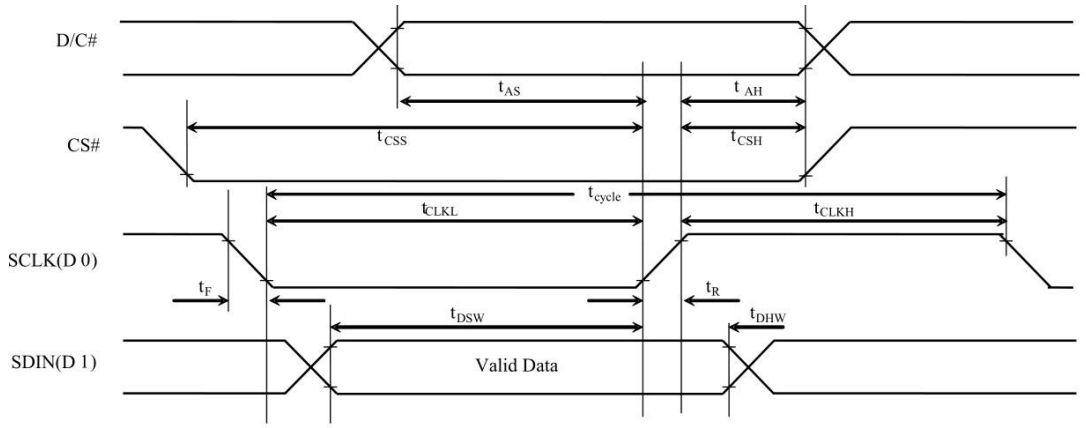


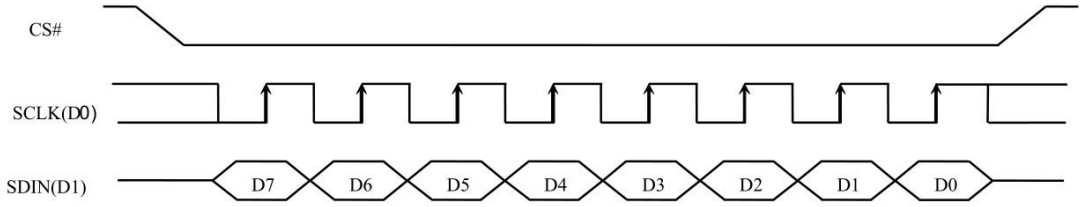
Read Cycle

7.5.2 4-Wire Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V~3.5V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	20	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	25	-	-	ns
t_{CLKL}	Clock Low Time	30	-	-	ns
t_{CLKH}	Clock High Time	30	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns





7.5.3 IIC Serial Interface Timing Characteristics

Conditions:

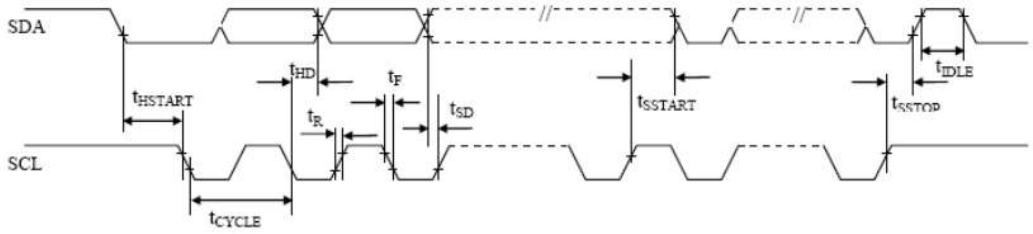
V_{DD} - V_{SS} = V_{DD} - V_{SS} = 1.65V to 3.3V

T_A = 25°C

I^2C Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I^2C interface Timing characteristics



7.5.4 6800 8bits Interface Timing Characteristics

Refer to IC Spec.: SSD1315

8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

Power ON sequence:

1.Power ON VDD

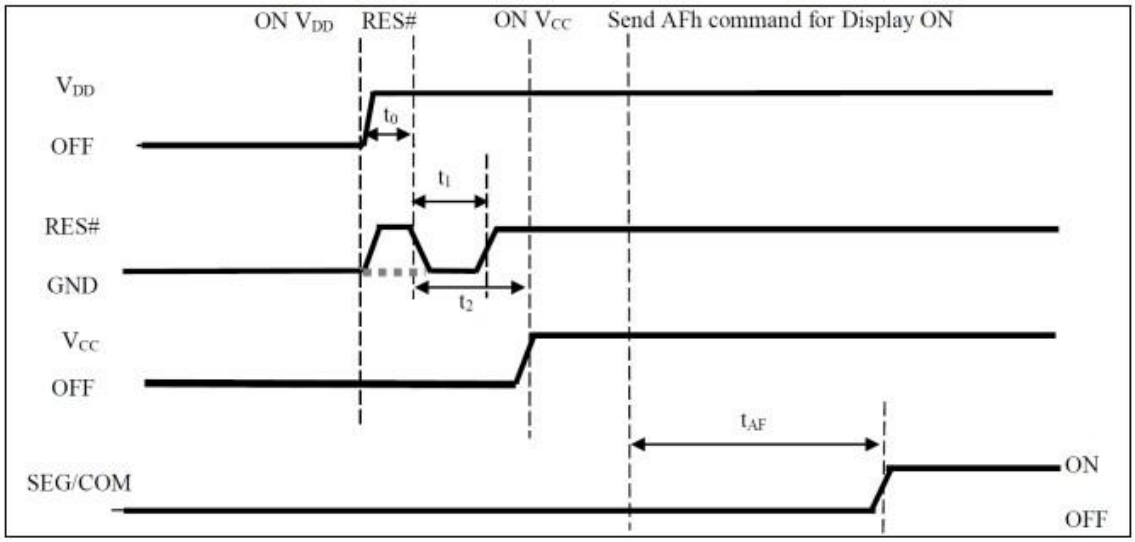
2.After VDD become stable, wait at least 20ms (t0), set RES# pin LOW (logic

3.low) for at least 3us (t1) (4) and then HIGH (logic high).

After set RES# pin LOW (logic low), wait for at least 3us (t2). Then Power ON VCC. (1)

4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (tAF).

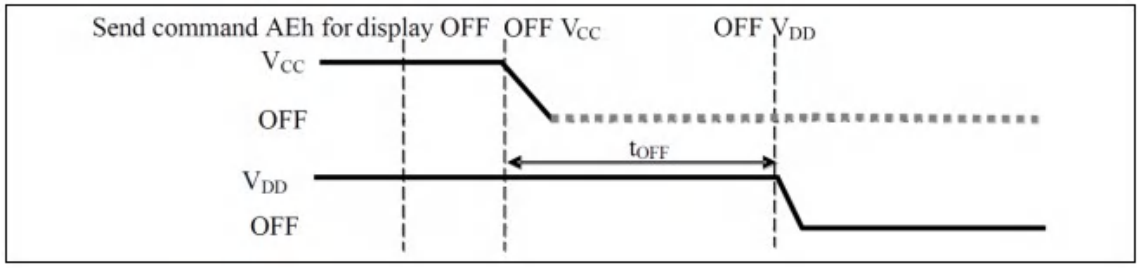
The Power ON Sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF VCC. (1), (2)
3. Power OFF VDD after tOFF. (4) (where Minimum tOFF=0ms, typical tOFF=100ms)

The Power OFF Sequence



Note:

(1) VCC should be kept float (i.e. disable) when it is OFF.

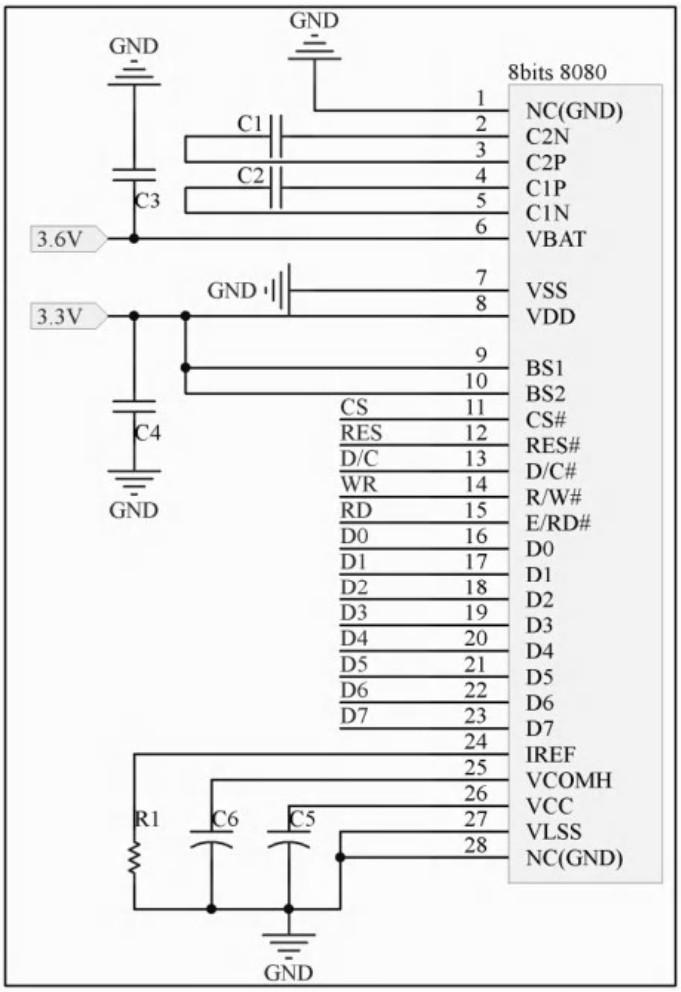
(2) Power Pins (VDD, VCC) can never be pulled to ground under any circumstance.

(3) The register values are reset after t1.

(4) VDD should not be Power OFF before VCC Power OFF.

8.2 APPLICATION CIRCUIT

8.2.1 This circuit is for 8080 8bits interface, Charge pump application.



Recommended components:

C5、C6：4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

C3、C4：1uF/16V(0603)

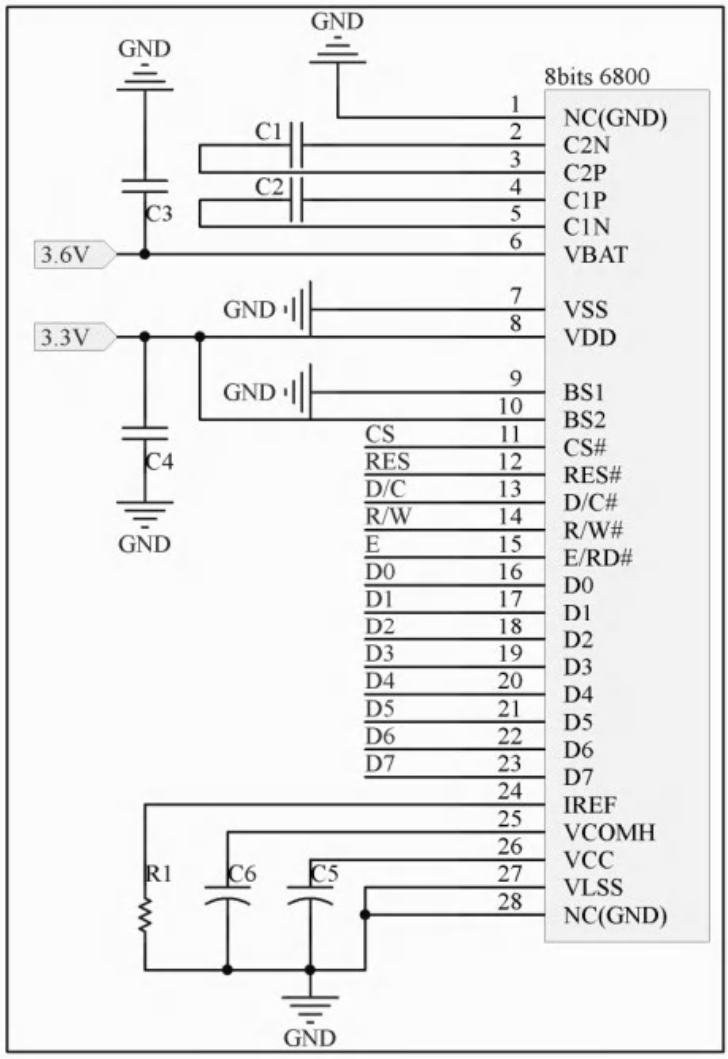
C1、C2：1uF/16V(0603)

R1：620Kohm 1%(0603)

Note: Vbat is also can be set 3.3V and connect VDD together.

For charge pump mode, VCC not need to connect external voltage supplier.

8.2.2 This circuit is for 6800 8bits interface, Charge pump application.



Recommended components:

C5、C6：4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

C3、C4：1uF/16V(0603)

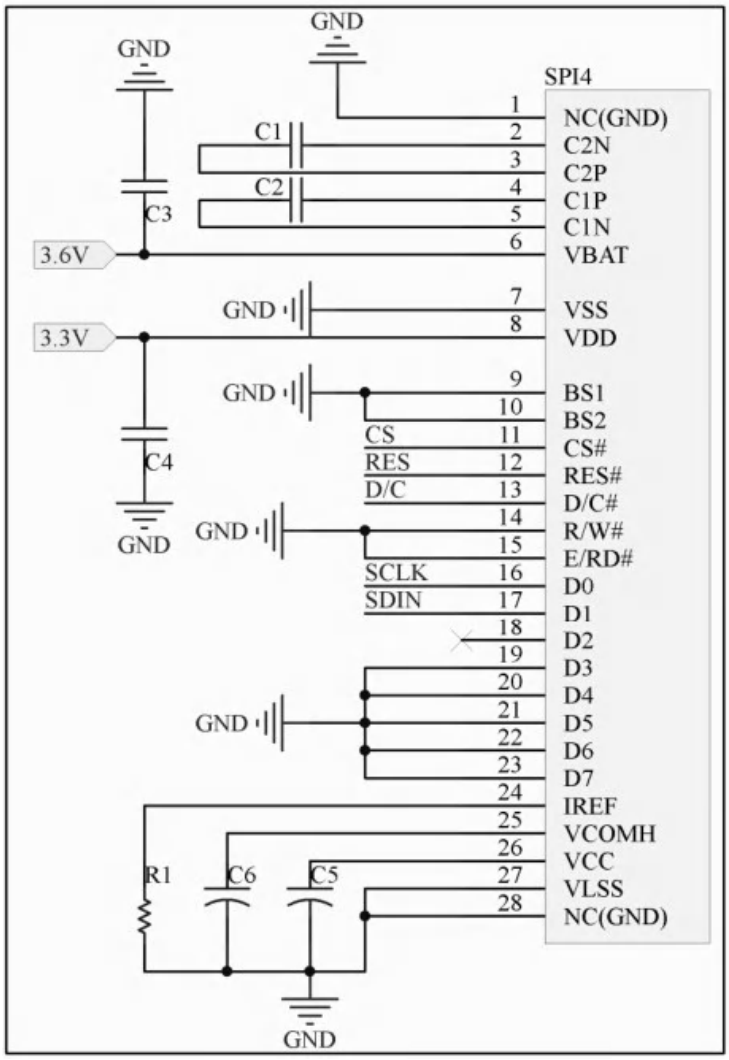
C1、C2：1uF/16V(0603)

R1：620Kohm 1%(0603)

Note: Vbat is also can be set 3.3V and connect VDD together.

For charge pump mode, VCC not need to connect external voltage supplier.

8.2.3 This circuit is for 4 wire SPI interface, Charge pump application.



Recommended components:

C5、C6：4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

C3、C4：1uF/16V(0603)

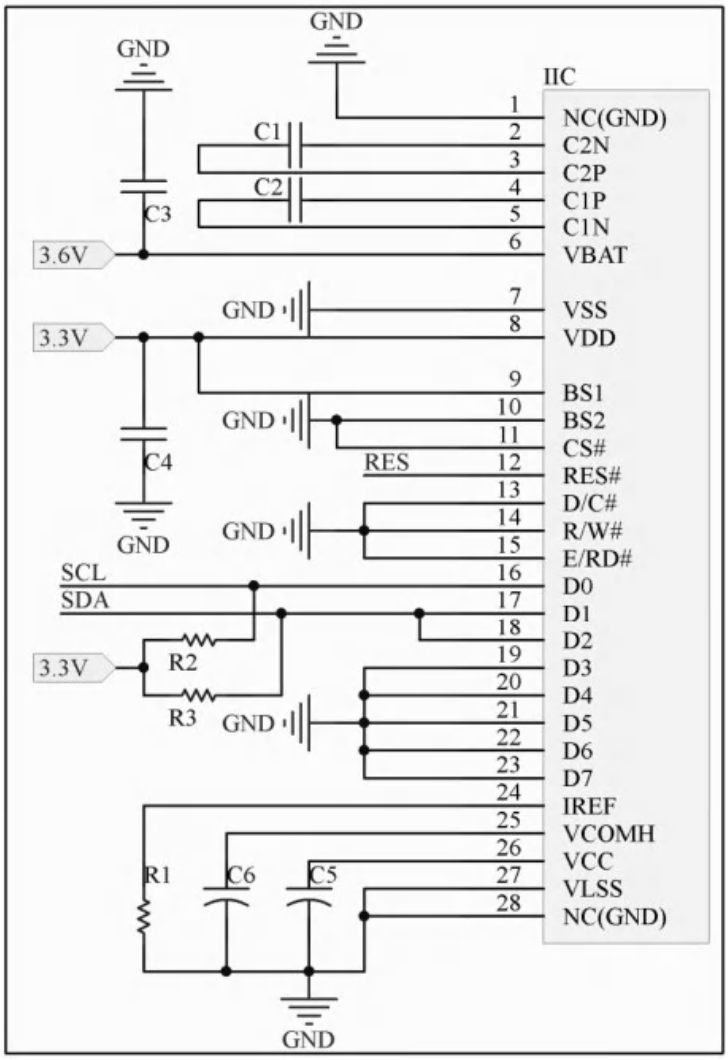
C1、C2：1uF/16V(0603)

R1：620Kohm 1%(0603)

Note: Vbat is also can be set 3.3V and connect VDD together.

For charge pump mode, VCC not need to connect external voltage supplier.

8.2.4 This circuit is for IIC interface, Charge pump application.



Recommended components:

C5、C6：4.7uF/25V(Tantalum type) or VISHAY (572D475X0025A2T)

C3、C4：1uF/16V(0603)

C1、C2：1uF/16V(0603)

R2、R3：10K(0603) (Should be adjusted based on IIC waveform)

R1：620Kohm 1%(0603)

Note: Vbat is also can be set 3.3V and connect VDD together.

For charge pump mode, VCC not need to connect external voltage supplier.

8.3 Initial code

```
void Initial_ic(void)
{
Write_Command(0xAE); //Display Off
Write_Command(0xD5); //SET DISPLAY CLOCK
Write_Command(0x80); //105HZ
Write_Command(0xA8); //Select Multiplex Ratio
Write_Command(0x2F); //Default => 0x2F (1/48 Duty)
Write_Command(0xD3); //Setting Display Offset
Write_Command(0x00); //00H Reset
Write_Command(0x40); //Set Display Start Line
Write_Command(0x8D); //Set Charge Pump
//Write_Command(0x10); //Disable Charge Pump
Write_command(0x14); //Enable Charge Pump
Write_command(0xAD); // Internal IREF Setting
Write_command(0x20); // Disable internal IREF
//Write_command(0x30); // Enable internal IREF
Write_Command(0xA1); //Set Segment Re-Map Default
Write_Command(0xC8); //Set COM Output Scan Direction
Write_Command(0xDA); //Set COM Hardware Configuration
Write_Command(0x12); //Alternative COM Pin
Write_Command(0x81); //Set Contrast Control
Write_Command(0X7D);
Write_Command(0xD9); //Set Pre-Charge period
Write_Command(0x22);
Write_Command(0xDB); //Set Deselect Vcomh level
```

```
Write_Command(0x00);
Write_Command(0xA4); //Entire Display ON
Write_Command(0xA6); //Set Normal Display
Clear_Ram();
Write_Command(0xAF); //Display ON
}
void Clear_Ram (void)
{
int i,j;
for(i=0;i<8;i++)
{
Write_Command (0xb0+i); //Set Page
Write_Command (0x00); //Lower Column Address
Write_Command (0x10); //Higher Column Address
for(j=0;j<128;j++)
{
data_out(0x00);
}
}
```

8.4 COMMAND TABLE

Refer to IC Spec.: SSD1315

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	80°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~80°C (-40°C /30min; transit /3min; 80°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

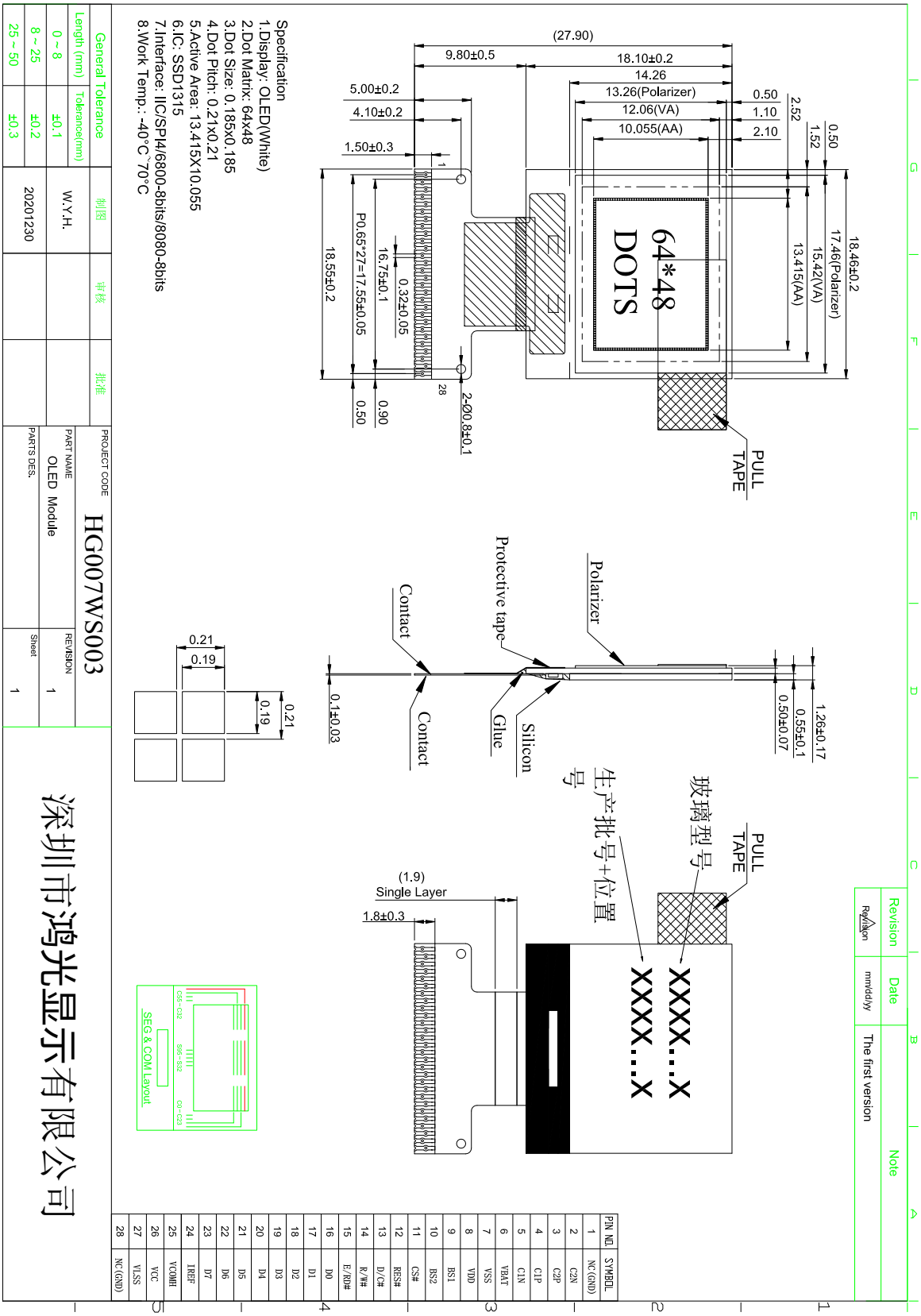
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. The degradation of Polarizer are ignored for item 1, 3 & 5.

Evaluation criteria

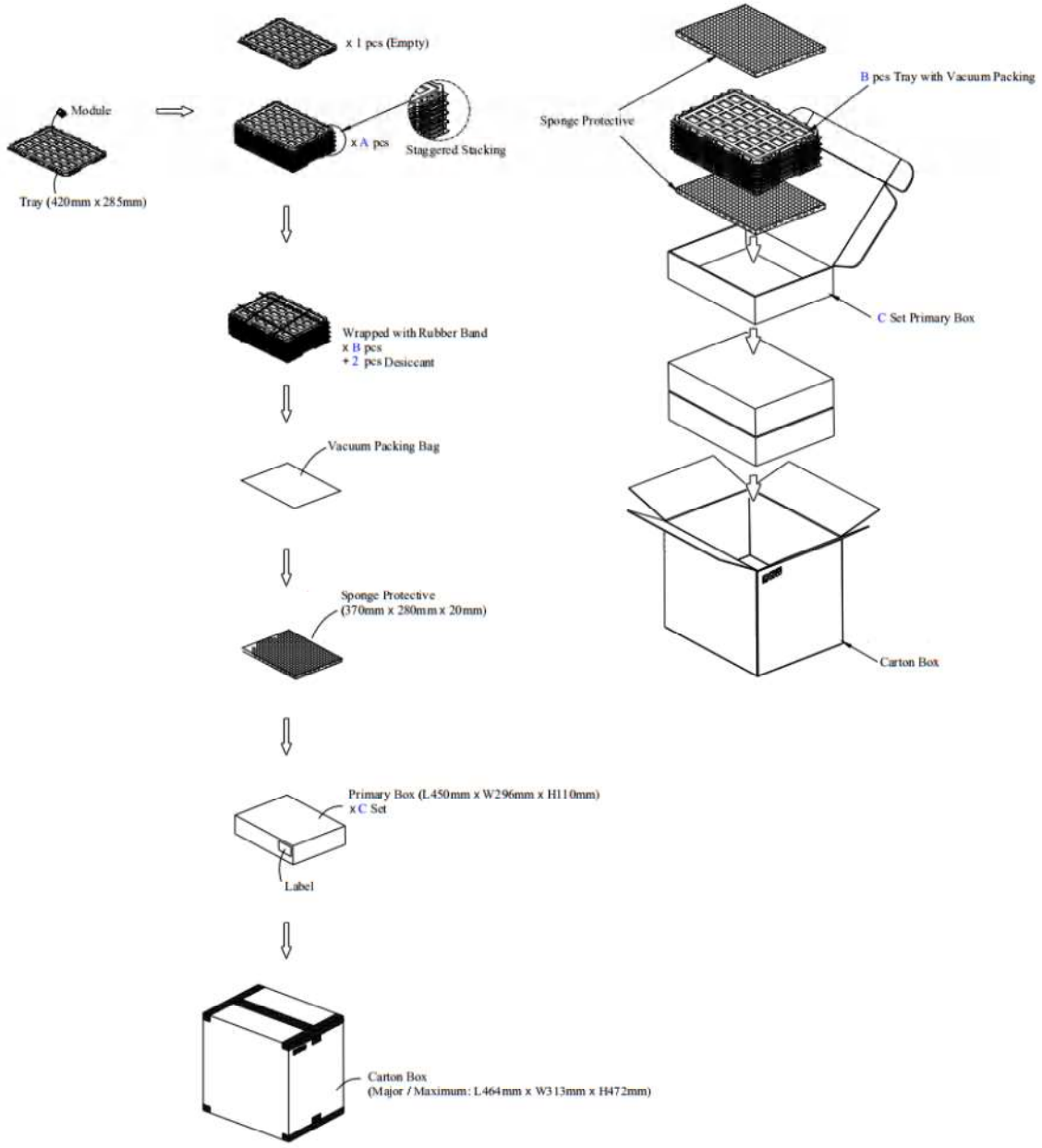
1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



PIN NO.	SYMBOL
1	NC (GND)
2	C2N
3	C2P
4	C1P
5	C1N
6	VBAT
7	VSS
8	VDD
9	BS1
10	BS2
11	CS#
12	RES#
13	D/C#
14	R/W#
15	E/RD#
16	D0
17	D1
18	D2
19	D3
20	D4
21	D5
22	D6
23	D7
24	IREF
25	VCOMH
26	VCC
27	VLSS
28	NC (GND)

11. PACKING SPECIFICATION



Item		Quantity	
Module		4680	**per Carton Box**
Module		1170	**per Primary Box**
Holding Trays	**(A)**	**15**	**per Primary Box**
Total Trays	**(B)**	**16**	**per Primary Box (Including 1 Empty Tray)**
Primary Box	**(C)**	**1~4**	**per Carton (4 as Major / Maximum)**

12. OUTGOING INSPECTION PROVISION

1. 抽样方法 / SAMPLING METHOD

(1) MIL-STD-1916 / 验证水平 level III / 正常检验 / 单次样品检验
MIL-STD-1916 / inspection level III / normal inspection / single sample inspection

(2) 主要缺陷 Level III；次要缺陷 Level II
Major Level III ; Minor Level II

MIL-STD-1916 樣本代字對照表							
批量	驗證水準（VL）						
	VII	VI	V	IV	III	II	I
2～170	A	A	A	A	A	A	A
171～288	A	A	A	A	A	A	B
289～544	A	A	A	A	A	B	C
545～960	A	A	A	A	B	C	D
961～1632	A	A	A	B	C	D	E
1633～3072	A	A	B	C	D	E	E
3073～5440	A	B	C	D	E	E	E
5441～9216	B	C	D	E	E	E	E
9217～17408	C	D	E	E	E	E	E
17409～30720	D	E	E	E	E	E	E
≧30721	E	E	E	E	E	E	E

样本代字 (CL)	验证水平(VL)							
	T	VII	VI	V	IV	III	II	I
	样本大小							
A	3072	1280	512	192	80	32	12	5
B	4096	1536	640	256	96	40	16	6
C	5120	2048	768	320	128	48	20	8
D	6144	2560	1024	384	160	64	24	10
E	8192	3072	1280	512	192	80	32	12

2. 检验条件 / INSPECTION CONDITION

检查和测量在下列条件下进行的，除非另有规定。

The inspection and meaurement are performed under the following conditions, unless otherwise specified.

温度 / Temperature: 25±5° C

湿度 / Humidity: 50±10%R.H.

压力 / Pressure: 860~1060hPa (mbar)

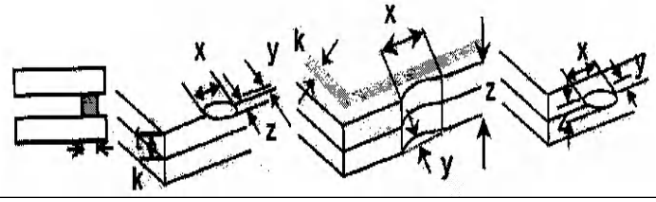
检验员拿的面板和眼睛之间的距离 / Distance between the panel and eyes of the inspector≧30cm

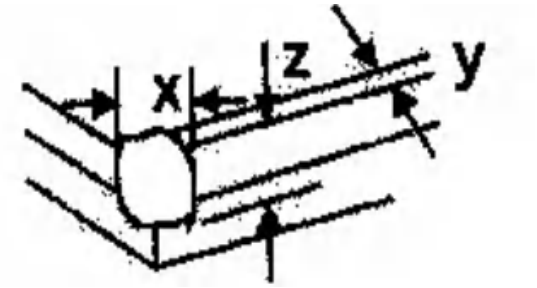
3. 质量检验规格 / SPECIFICATION FOR QUALITY CHECK

3.1 缺陷分类 / DEFECT CLASSIFICATION

严重度 Severity	检验项目 Inspection Item	缺陷 Defect	备注 Remark
主要缺陷 Major Defect	1. 面板 Panel	(1) 无显示 Non-displaying	
		(2) 线缺陷 Line defects	
		(3) 故障 Malfunction	
		(4) 玻璃破损 Glass cracked	
	2. 软板 Film	(1) 软板尺寸超规 Film dimension out of specification	不能组装 Can not be assembled
	3. 尺寸 Dimension	(1) 外形尺寸超规 Outline dimension out of specification	
次要缺陷 Minor Defect	1. 面板 Panel	(1) 玻璃刮伤 Glass scratch	外观缺陷 Appearance defect
		(2) 玻璃切割异常 Glass cutting NG	
		(3) 玻璃崩边、崩角 Glass chip	
	2. 偏光板 Polarizer	(1) 偏光板刮伤 Polarizer scratch	
		(2) 表面污渍 Stains on surface	
		(3) 偏光板气泡 Polarizer bubbles	
	3. 显示 Displaying	(1) 暗点、亮点、脏污 Dim spot、Bright spot、dust	
	4. 软板 Film	(1) 损伤 Damage	
		(2) 异物 Foreign material	

3.2 出货规格 / OUTGOING SPECIFICATION

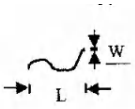
<table>
<tr><th>项目
Item</th><th>描述
Description</th><th>标准
Criterion</th><th>允收水平
AQL</th></tr>
<tr><td rowspan="3">I. 面板
Panel</td><td>1.玻璃刮伤
Glass scratch</td><td>
<table>
<tr><th>寬 / Width (mm) W</th><th>長 / Length (mm) L</th><th>容許個數 number of pieces permitted</th></tr>
<tr><td>W≦0.03</td><td>忽略
Ignore</td><td>忽略
Ignore</td></tr>
<tr><td>0.03 < W≦0.05</td><td>L≦1</td><td>1</td></tr>
<tr><td>0.05 < W</td><td>------</td><td>無
None</td></tr>
<tr><td>顯示區外
beyond A.A.</td><td>------</td><td>忽略
Ignore</td></tr>
</table>
</td><td>次要
Minor</td></tr>
<tr><td>2. 玻璃破损
Glass crack</td><td>(1) 裂纹 / Crack
扩展裂纹是不能接受的。
Propagation crack is not acceptable.
  </td><td>主要
Major</td></tr>
<tr><td>3. 玻璃崩边、崩角
Glass chip</td><td>Symbols Define:
x: Chip length y: Chip width z: Chip thickness
k: Seal width t: Glass thickness a: OLED side length
L: Electrode pad length:
3.1 General glass chip :
3.1.1 Chip on panel surface and crack between panels:
  </td><td>次要
Minor</td></tr>
</table>

<table>
<tr><th>项目
Item</th><th>描述
Description</th><th>标准
Criterion</th><th>允收水平
AQL</th></tr>
<tr><td rowspan="2">I. 面板
Panel</td><td>3. 玻璃崩边、崩角
Glass chip</td><td>
<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is total length of each chip.
3.1.2 Corner crack:


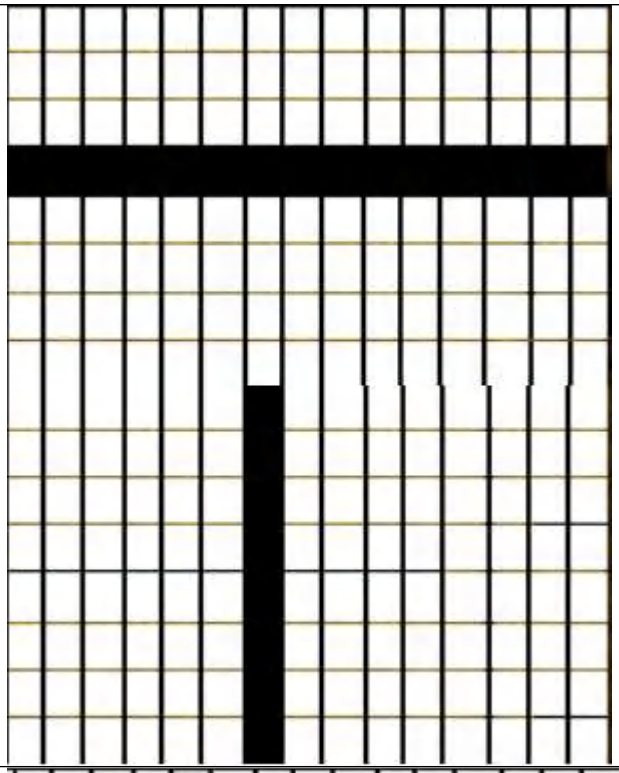
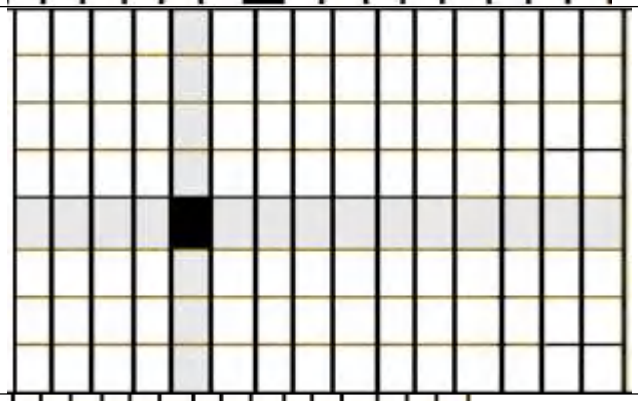
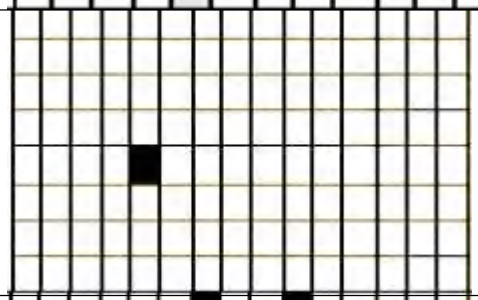
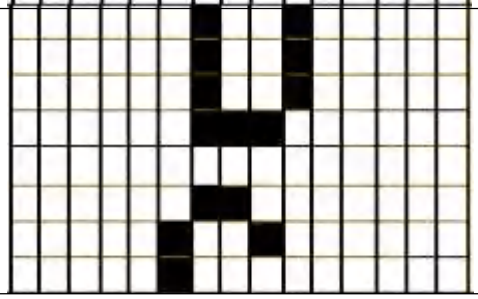
<table>
<tr><td>z: Chip thickness</td><td>y: Chip width</td><td>x: Chip length</td></tr>
<tr><td>Z≦1/2t</td><td>Not over viewing area</td><td>x≦1/8a</td></tr>
<tr><td>1/2t＜z≦2t</td><td>Not exceed 1/3k</td><td>x≦1/8a</td></tr>
</table>
⊙If there are 2 or more chips, x is the total length of each chip.
</td><td>次要
Minor</td></tr>
<tr><td>4. 尺寸
Dimension</td><td>请参阅图纸的规范。
Refer to the drawing of the spec</td><td>主要
Major</td></tr>
<tr><td rowspan="2">II. 偏光板
Polarizer</td><td>1. 刮伤
Scratch</td><td>点状按照“项目 II-3 偏光板气泡”的标准。
Spot type in accordance with the criteria of “Item II-3. Polarizer bubble”.
线状按照“项目 I-1 玻璃刮伤”的标准。
Line type in accordance with the criteria of “Item I-1. Glass scratch”.</td><td>次要
Minor</td></tr>
<tr><td>2. 表面污渍
Stains on surface</td><td>表面污渍无法用软布或类似的清洁物轻轻擦拭去除。
Stains cannot be removed even when wiped lightly with a soft cloth or similar cleaning.</td><td>次要
Minor</td></tr>
</table>

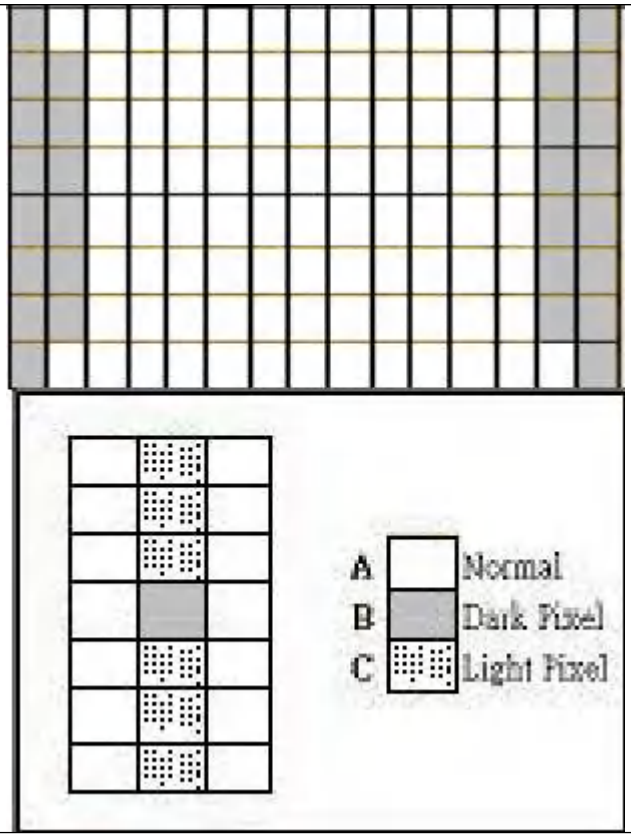
	3. 偏光板气泡 Polarizer bubble	(mm) 尺寸 Size / 容许个数 number of pieces permitted Φ≦0.2 / 忽略 Ignore 0.2＜Φ≦0.5 / 3 0.5＜Φ≦1 / 2 1＜Φ / 0 Total qty / 3 显示区外 beyond A.A. / 忽略 Ignore	次要 Minor

项目 Item	描述 Description	标准 Criterion	允收水平 AQL
III. 显示 Displaying	1. 耗电 Power consumption	该模块的工作电流消耗不应超出产品规格书的规范。 The module operating current consumption should not go beyond the standard indicated in Product Specification	主要 Major
	2. 像素尺寸 Pixel size	显示像素的尺寸的公差应规格的±25%之内。 The tolerance of display pixel dimension should be within ±25% of specification.	次要 Minor
	3. 颜色 Color	依据产品规格。 Refer to the product specification.	主要 Major
	4. 亮度 Luminance	依据产品规格。 Refer to the product specification.	主要 Major
	5. 暗点、亮点 、脏污 Dimming spot、Lighting spot、Dust	1. SIZE / Acceptable QTY Φ≦0.10 / Accept no dense 0.10＜Φ≦0.20 / 2 0.20＜Φ≦0.25 / 1 0.25＜Φ / 0)/2 D=(long diameter + short diameter)/2 像素暗点是不允许。 Pixel off is not allowed.	次要 Minor

<table>
<tr><th>项目
Item</th><th>描述
Description</th><th>标准
Criterion</th><th>允收水平
AQL</th></tr>
<tr><td>III. 显示
Displaying</td><td>5. 暗点、亮点 、脏污
Dimming spot、Lighting spot、Dust</td><td>2.
 

<table>
<tr><th>Length</th><th>Width</th><th>Acceptable Q TY</th></tr>
<tr><td>---</td><td>W≦0.02</td><td>Accept no dense</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≦2.5</td><td>0.03＜W≦0.05</td></tr>
<tr><td>---</td><td>0.05＜W</td><td>As round type</td></tr>
</table></td><td>次要
Minor</td></tr>
<tr><td rowspan="3">IV. 软板
Film</td><td>1. 尺寸
Dimension</td><td>软板尺寸超规。
Film dimension out of Spec.</td><td>主要
Major</td></tr>
<tr><td>2. 损伤
Damage</td><td>破损；深刮伤；深折痕；深压痕或其他损害是不能接受的。
Crack; deep scratch; deep fold; deep pressure mark or other damage is not acceptable.</td><td>次要
Minor</td></tr>
<tr><td>3. 异物
Foreign material</td><td>导电异物附着在导线，软板和玻璃之间的异物是不能接受的。
Conductive foreign material sticking to the leads, foreign material between film and glass are not acceptable.</td><td>次要
Minor</td></tr>
<tr><td>V. 功能
Function</td><td>1.无显
Nodisplay</td><td>  </td><td>Major</td></tr>
</table>

	2. 缺划 Missing Line		Major
	3 像素点短路 Pixel Short		Major
	4 黑点短路 Darker Short		Major
	5 乱显 Wrong Display		Major

	6 显示不均 Un-uniform B/Ax100%<70% A/Cx100%<70%		Major

13. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

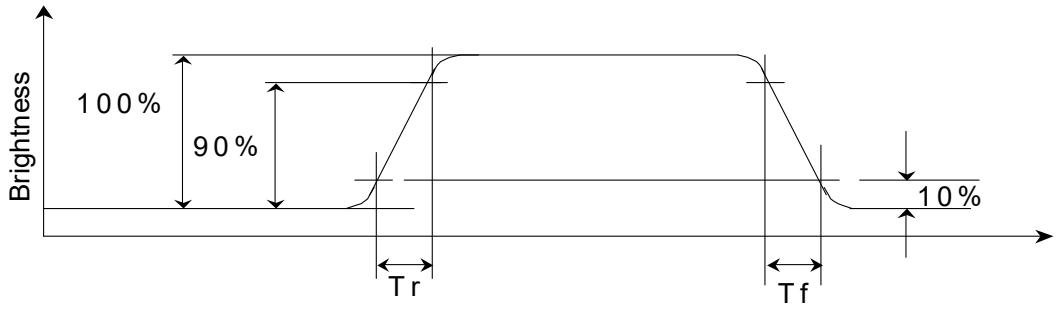


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

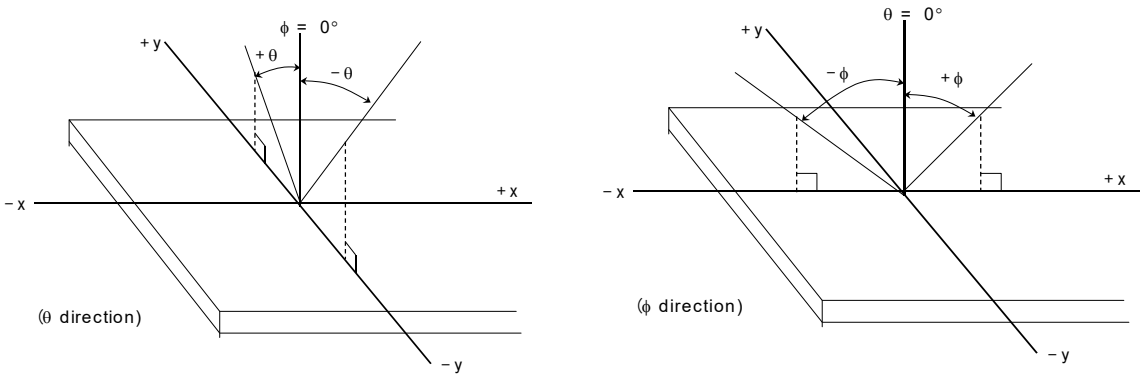
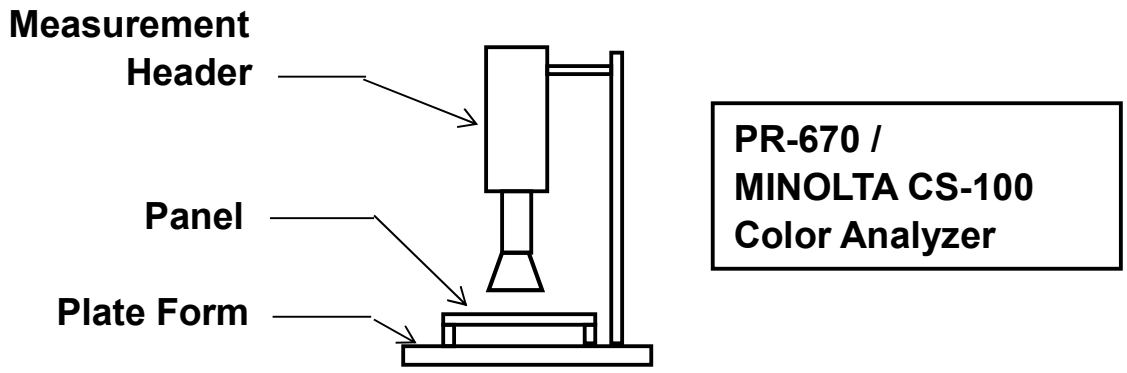


Figure 3 Viewing angle

APPENDIX 2: MEASUREMENT APPARATUS

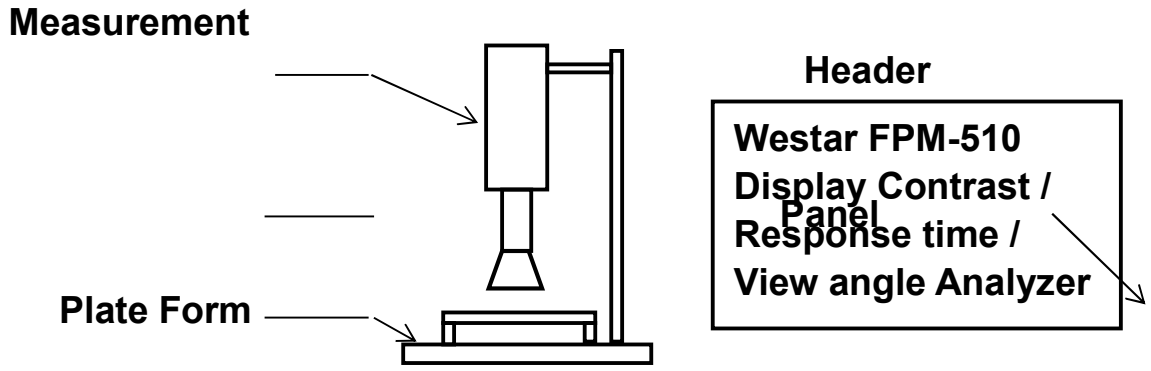
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-670, MINOLTA CS-100

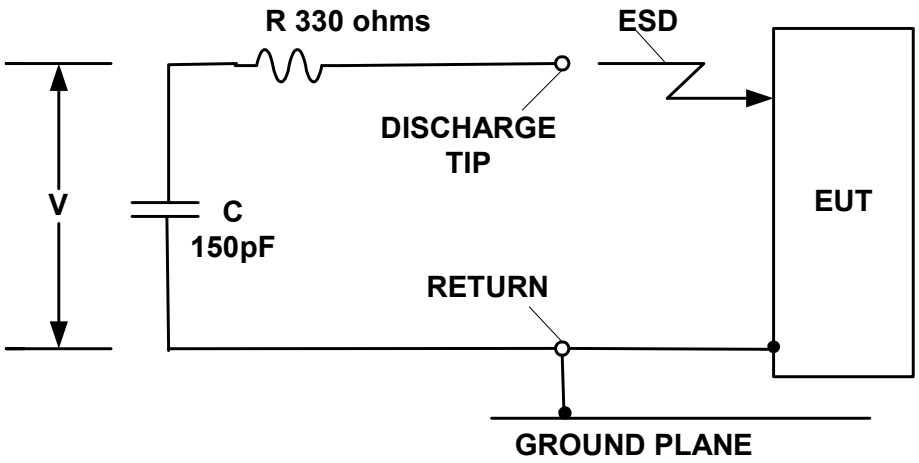


B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



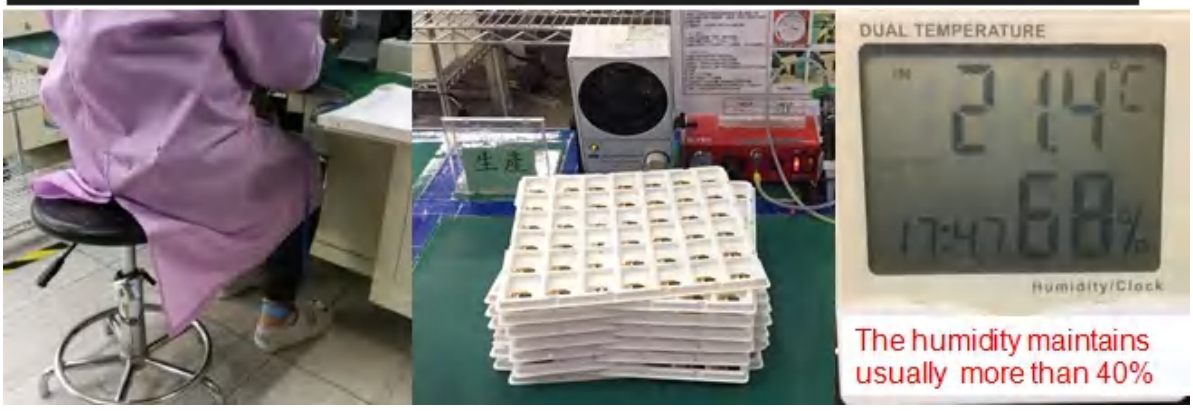
C. ESD ON AIR DISCHARGE MODE



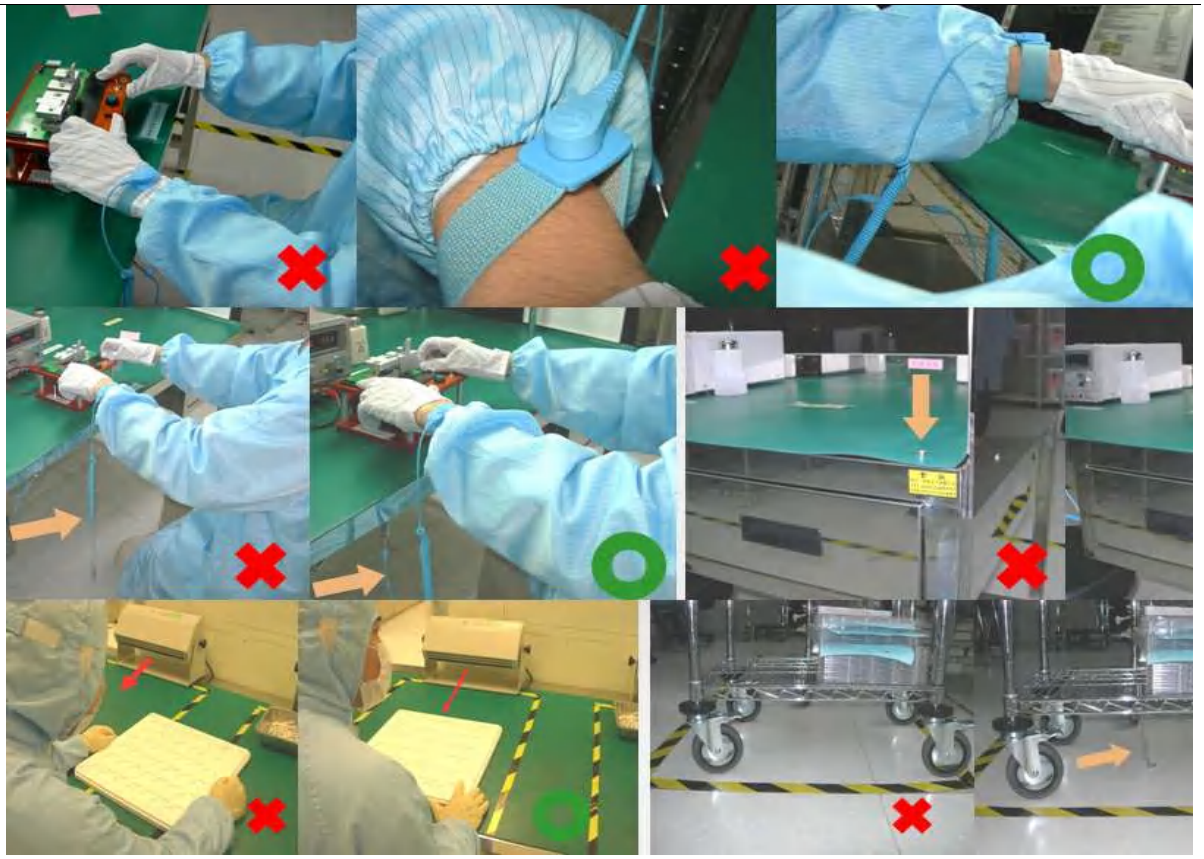
APPENDIX 3: PRECAUTIONS FOR USING THE OLED MODULE

Precautions for Handling

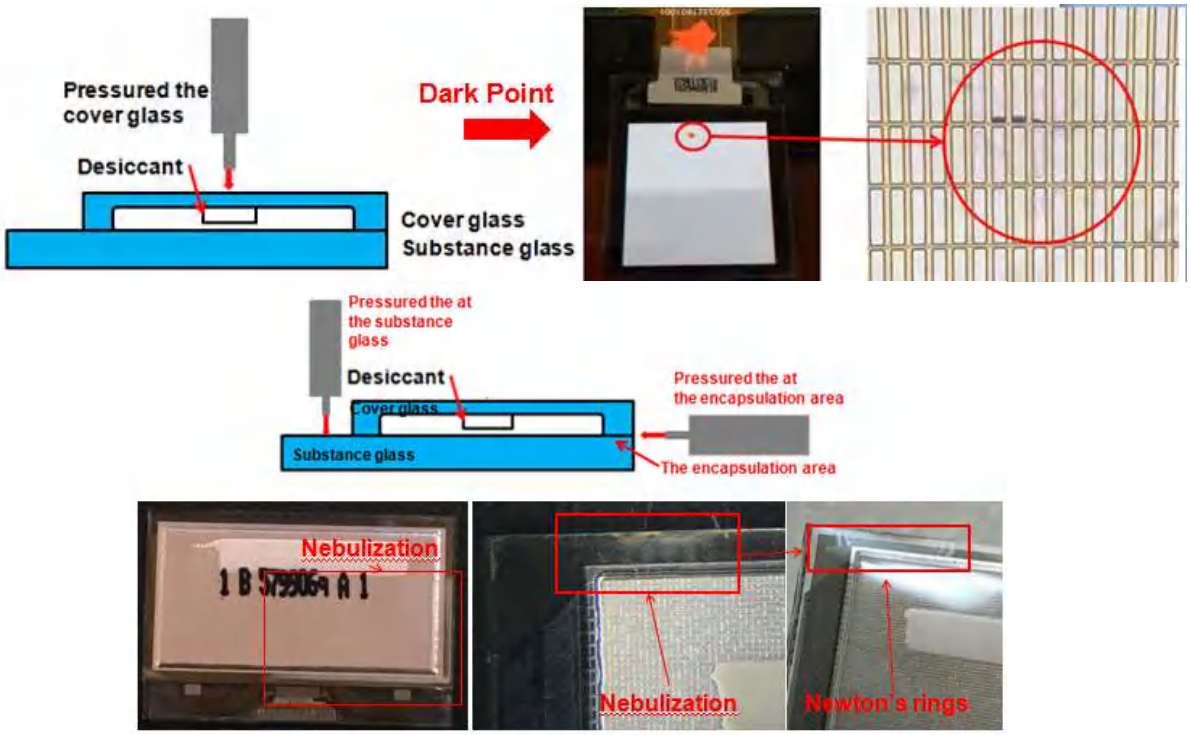
1. When handling the module, wear powder-free anti static rubber finger cots/ anti-static clothing, anti-static gloves ,antistatic wrist strap and anti-static shoes
   The environment should dispose the static elimination blower, anti-static pad, anti-static chair, and anti-static floor. The humidity maintains usually more than 40%



2. The OLED module is an electronic component and is subject to damage caused by Electro Static Discharge (ESD). And hence normal ESD precautions must be taken when handling it. Also, appropriate ESD protective environment must be administered and maintained in the production line. When handling and assembling the panel, wear an antistatic wrist strap with the alligator clip attached to the ground to prevent ESD damage on the panel. Antistatic wrist strap should touch human body directly instead of gloves. (See below photos).



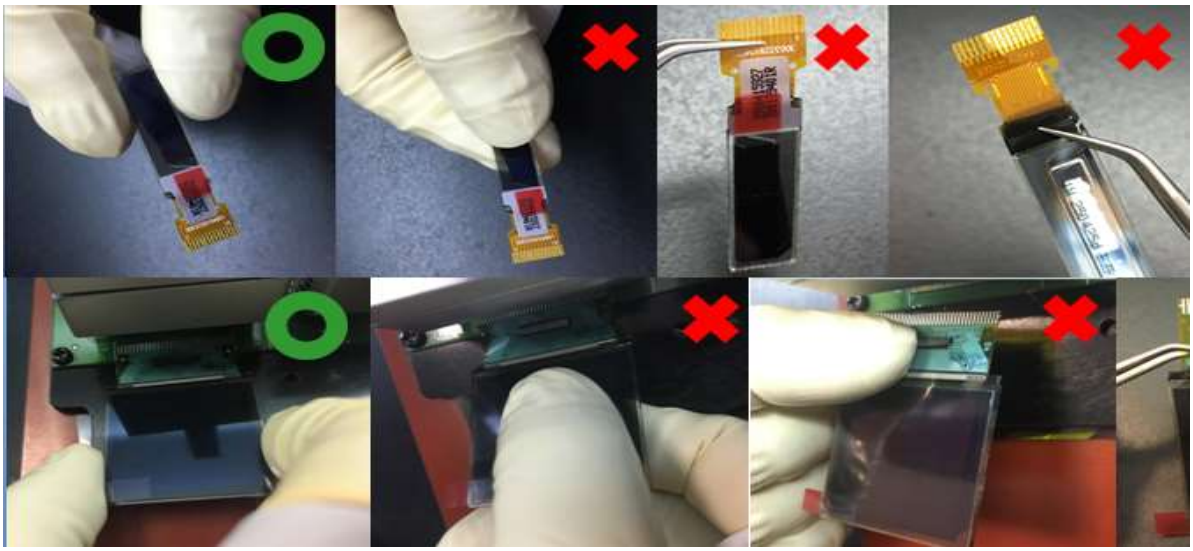
3. The OLED module is consisted of glass and film, and it should avoid pressure, strong impact, or being dropped from a high position.



4. Take out the panel one by one from the holding trays for assembly, and never put the panel on top of another one to avoid the scratch.

5. Avoid jerk and excessive bend on TAB/FPC/COF, and be careful not to let foreign matter or bezel damage the film.

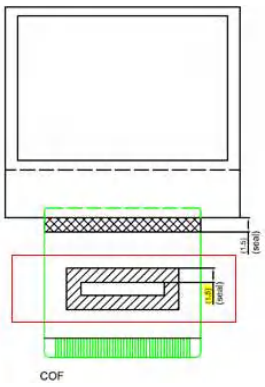
6. When handling and assembling the module (panel + IC), grab the panel, not the TAB/FPC/COF.

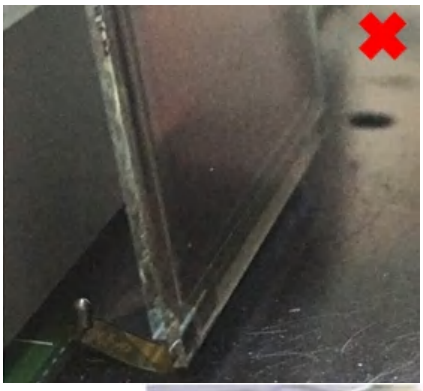


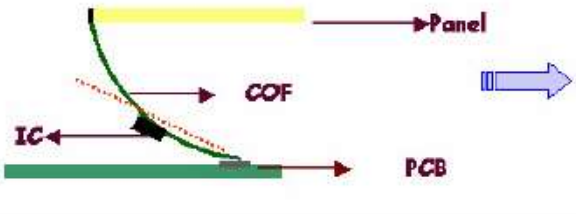
7. Use the tweezers to open the clicks on the connector of PCB before the insertion of FPC/COF, and click them back in. Once the FPC/COF sits properly in the connector, use the tweezers to avoid the damages.

8. Please do not bend the film near the substrate glass. It could cause film peeling and TAB/FPC/COF damage. For TAB, It should bend the slit area as actual OLED it is. For FPC or COF, it is suggested to follow below pictures for instruction (distance between substrate glass and bending area >1.5mm; R>0.5mm).

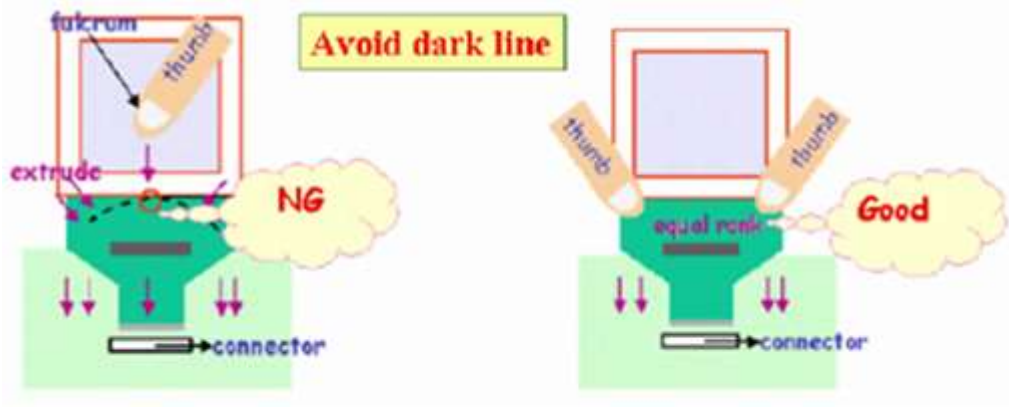
9. Avoid bending the film at IC bonding area. It could damage the IC ILB bonding. It should avoid bending the IC seal area. Please keep the bending distance >1.5mm.



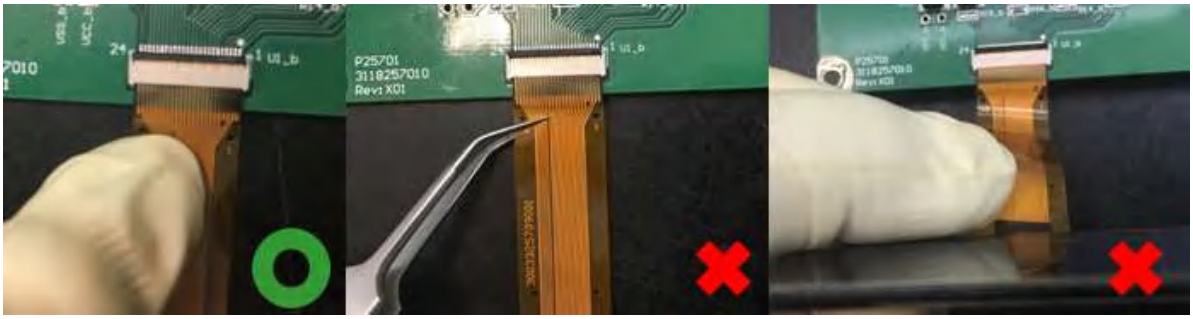




Use finger to insert COF /FPC into the connector when assembling the panel. Please refer to the photo.



COF: Use both thumbs



10. Do not wipe the pin of film and polarizer with the dry or hard materials that will damage the surface. When cleaning the display surface, use the soft cloth with solvent, IPA or alcohol, to clean.

11. Protection film is applied to the surface of OLED panel to avoid the scratch. Please remove the protective film before assembling it. If the OLED panel has been stored for a long time, the residue adhesive material of the protective film may remain on the display surface after remove the protective film. Please use the soft cloth with solvent, IPA or alcohol, to clean.

12. When hand or hot-bar soldering TAB/FPC onto PCB, make sure the temperature and timing profiles to meet the requirements of soldering specification (the specification depends on the application or optimized by customer) to prevent the damage of IC pins by inappropriate soldering, and also avoid the high temperature to damage the Organic light-emitting materials.

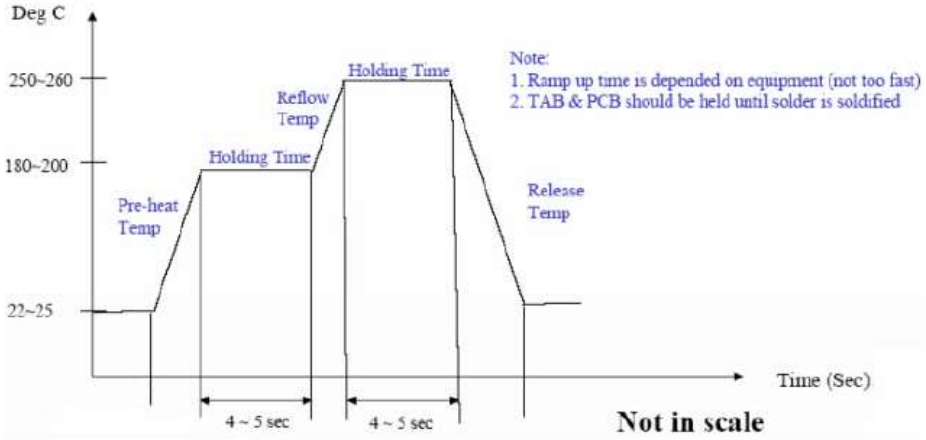
13. Solder residues arise from soldering process have to be cleaned up thoroughly before the module assembly.

14. Use the voltage and current settings listed in the specification to do the function test after the module assembly.

15. Suggestion for soldering process:

i. TAB Lead- free soldering hot bar process

1. Use pulse heated bonding tool equipment
2. Material: Sn/Ag/Cu lead-free solder paste with typical 25um thickness on PCB pad. The TAB pin size and shape may be different, please base on the production line to adjust the thickness of PCB pad and temperature. S
3. Bonding Force:--4kg per centimeter square as the starting point.
4. Suggested bonding tool temperature & time profile is as below for reference. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.



ii. TAB Lead- free soldering wire process

In case of manual soldering (Lead- free solder wire)

1. Solder wire contact iron directly: 280±5° C at 3-5secs
2. Solder wire contact TAB lead directly (near iron but not contact): 380±5 ° C, 3-5secs
3. Since there are differences in TAB soldering pins, soldering technicians' skills, mechanism…etc., the soldering conditions must be adequately tuned.

iii. High temperature will result in rapid heat conduction to IC and might cause damage to IC, so please keep the temperature below 380° C. Also, avoid damaging the polyimide and solder resist which might take place at high temperatures. Refold cycles base on the de-soldering status, if the plating of pin was damaged, it can not be used again.

Precautions for Electrical

1. Design using the settings in the specification

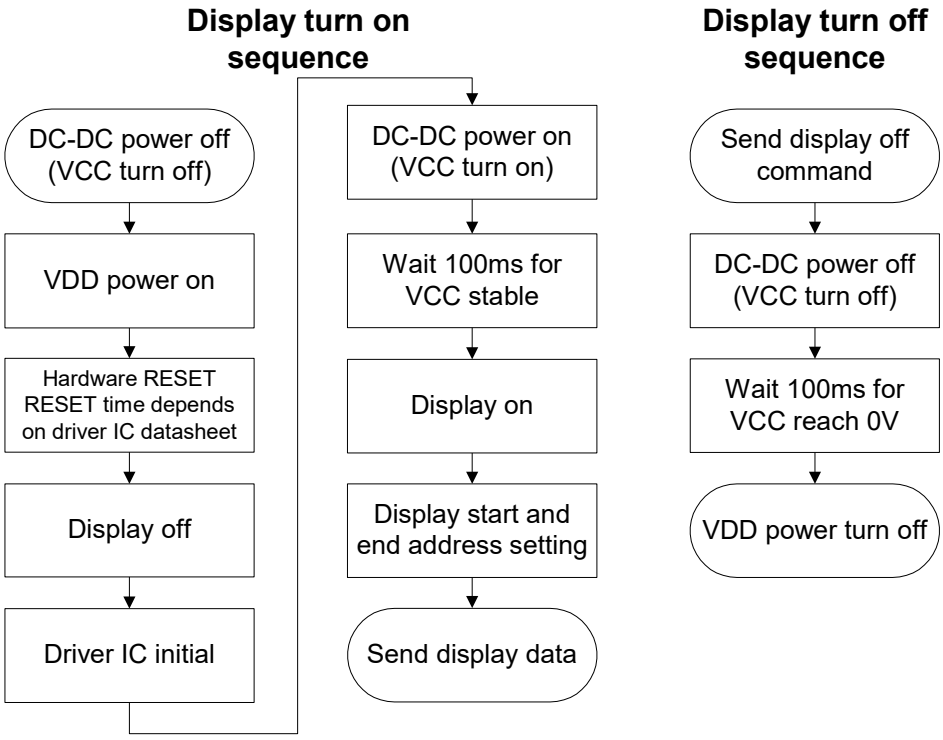
It is very important to design and operate the panel using the settings listed in the specification. It includes voltage, current, frame rate and duty cycle... etc. Operation the OLED outside the range of the specification should be entirely avoided to ensure proper operation of the OLED.

2. Maximum Ratings

To ensure the proper operation of the panel, never design the panel with parameters running over the maximum ratings listed in the specification. Also the logic voltages such as VIL and VIH have to be within the specified range in the specification to prevent any improper operation of the panel.

3. Power on/off procedure

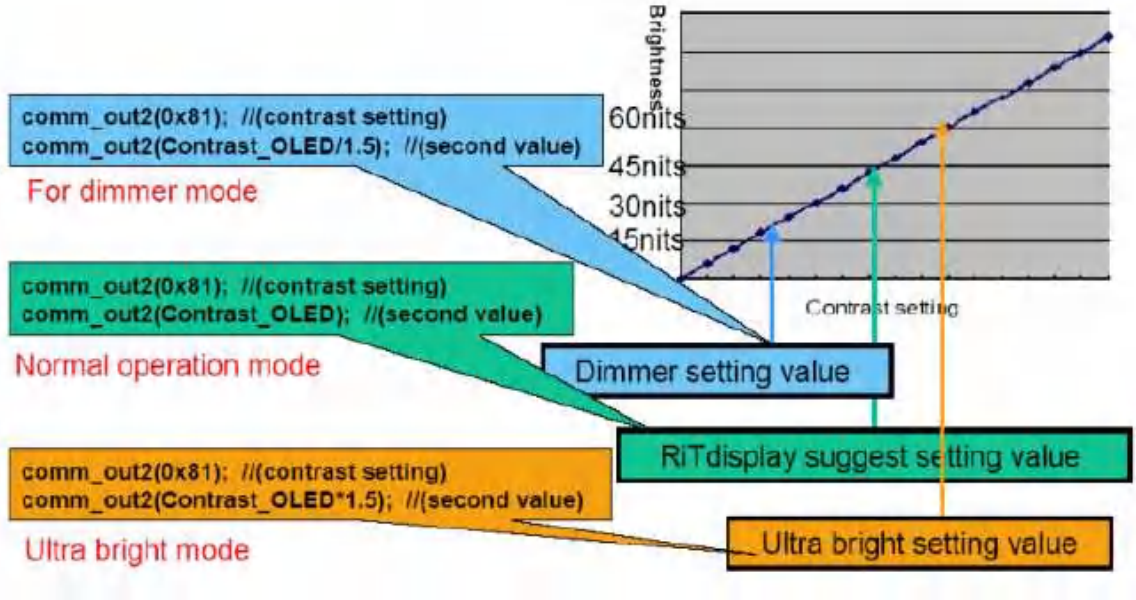
To avoid any inadvertent effects resulting from inappropriate power on/off operations, please follow the directions of power on/off procedure on page 13. Any operation that does not comply with the procedure could cause permanent damage of the IC and should be avoided. When the logic power is not on, do not activate any input signal. Abrupt shutdown of power to the module, while the OLED panel is on, would cause OLED panel malfunction.



4. Power savings

To save power consumption of the OLED, please use partial display or sleep mode when the panel is not fully activated. Also, if possible, make the black background to save power.

The OLED is a self-luminous device and a particular pixel cluster or image can be lit on via software control. So power savings can be achieved by partial display or dimming down the luminance. Depending on the application, the user can choose among Ultra Bright Mode, Normal Operation Mode, and Sleeping Mode. The power consumption is almost in directly proportion to the brightness of the panel, and also in directly proportion to the number of pixels lit on the panel. The customer can save the power by the use of black background and sleeping mode. One benefit from using these design schemes is the extension of the OLED lifetime.



5. Adjusting the luminance of the panel

Although there are a couple of ways to adjust the luminance of the panel, it is strongly recommended that the customer change the contrast setting to adjust the luminance of the panel. Adjusting voltages to achieve desired luminance is not allowed. Be aware that the adjustment of luminance would accompany the change of lifetime of the panel and its power consumption as well.

6. Residual Image (Image Sticking)

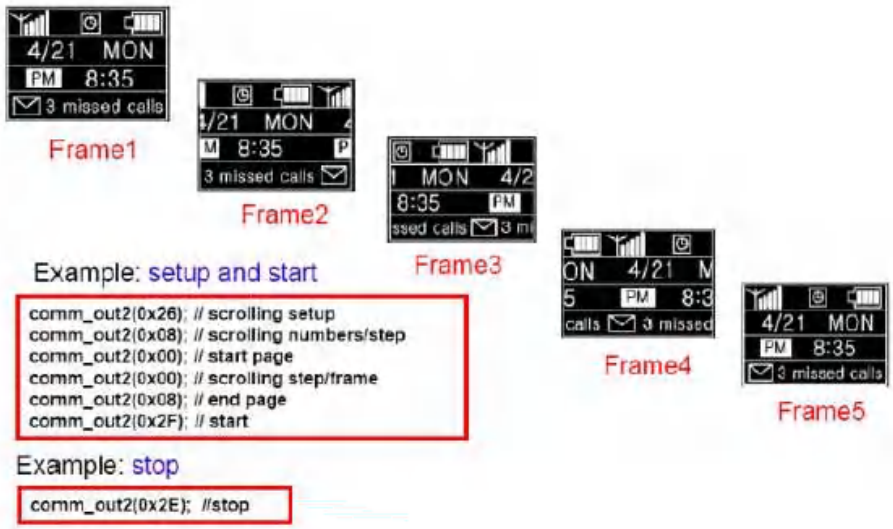
The OLED is a self-emissive device. As with other self-emissive device or displays consisting of self-emissive pixels, when a static image frozen for a long period of time is changed to another one with all-pixels-on background, residual image or image sticking is noticed by the human eye. Image sticking is due to the luminance difference or contrast between the pixels that were previously turned on and the pixels that are newly turned

on. Image sticking depends on the luminance decay curve of the display. The slower the decay, the less prominent the image sticking is. It is strongly recommended that the user employ the following four strategies to minimize image sticking.

1. Employ image scrolling or animation to even out the lit-on time of each and every pixel on the display, also could use sleeping mode for reduced the residual image and extend the power capacity.
2. Minimize the use of all-pixels-on or full white background in their application because when the panel is turned on full white, the image sticking from previously shown patterns is the most revealing. Black background is the best for power savings, greatest visibility, eye appealing, and dazzling displays.
3. Avoid displaying the characters or menu with high brightness level in a fix position for a long time or repeatedly. If necessary, using the auto fadeout technology.
4. If a static logo is used in the reliability test, change the pattern into its inverse (i.e., turn off the while pixels and turn on the previously unlit pixels) and freeze the inverse pattern as long as the original logo is used, so every pixel on the panel can be lit on for about the same time to minimize image sticking, caused by the differential turn-on time between the original and its reverse patterns.

Black Background

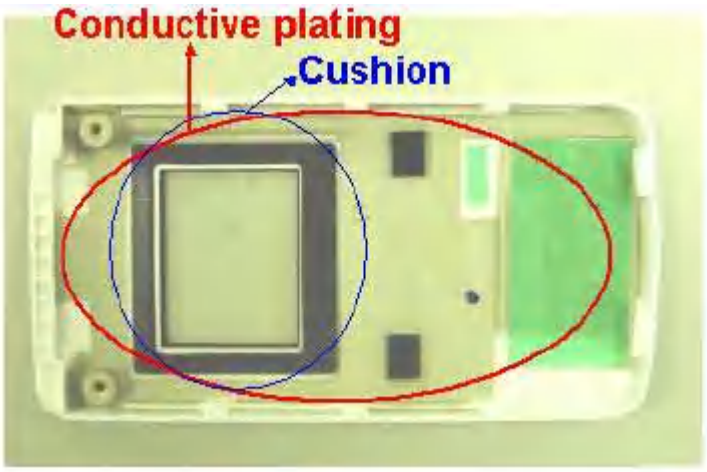
Scrolling example



Precautions for Mechanical

1. Cushion or Buffer tape on the cover glass

It is strongly recommended to have a cushion or buffer tape to apply on the panel backside and front side when assembling OLED panel into module to protect it from damage due to excessive extraneous forces.



It is recommended that a plating conductive layer be used in the housing for EMI/EMC protection. And, the enough space should be reserved for the IC placement if the IC thickness is thicker than the TAB film when customer design the PCB.

2. Avoid excessive bending of film when handling or designing the panel into the product

The bending of TAB/COF/FPC has to follow the precautions indicated in the specification, extra bending or excessive extraneous forces should be avoided to minimize the chances of film damage. If bending the film is necessary, please bend the designated bending area only. Please refer to items 8 and 9 of Precautions for Handling for more information.

Precautions for Storage and Reliability Test

1. Storage

Store the packed cartons or packages at 25° C±5° C, 55%±10%RH. Do not store the OLED module under direct sunlight or UV light. For best panel performance, unpack the cartons and start the production of the panels within six months after the reception of them.

2. Reliability Test

Supplier only guarantees the reliability of the OLEDs under the test conditions and durations listed in the specification.