SPECIFICATION

FOR

TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HL MODEL : HG101WX046

■**Preliminary Specification**

■**Final Specification**

Customer Confirmation column:

Approved by :_____Dept. :_____Data :_____

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Designed by	Checked by	Approved by

REVISION STATUS

Version	Revise Date	Page	Content	Modified by
V1.0	2022.08.30	-	First Issued.	M

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1. GENERAL DESCRIPTION

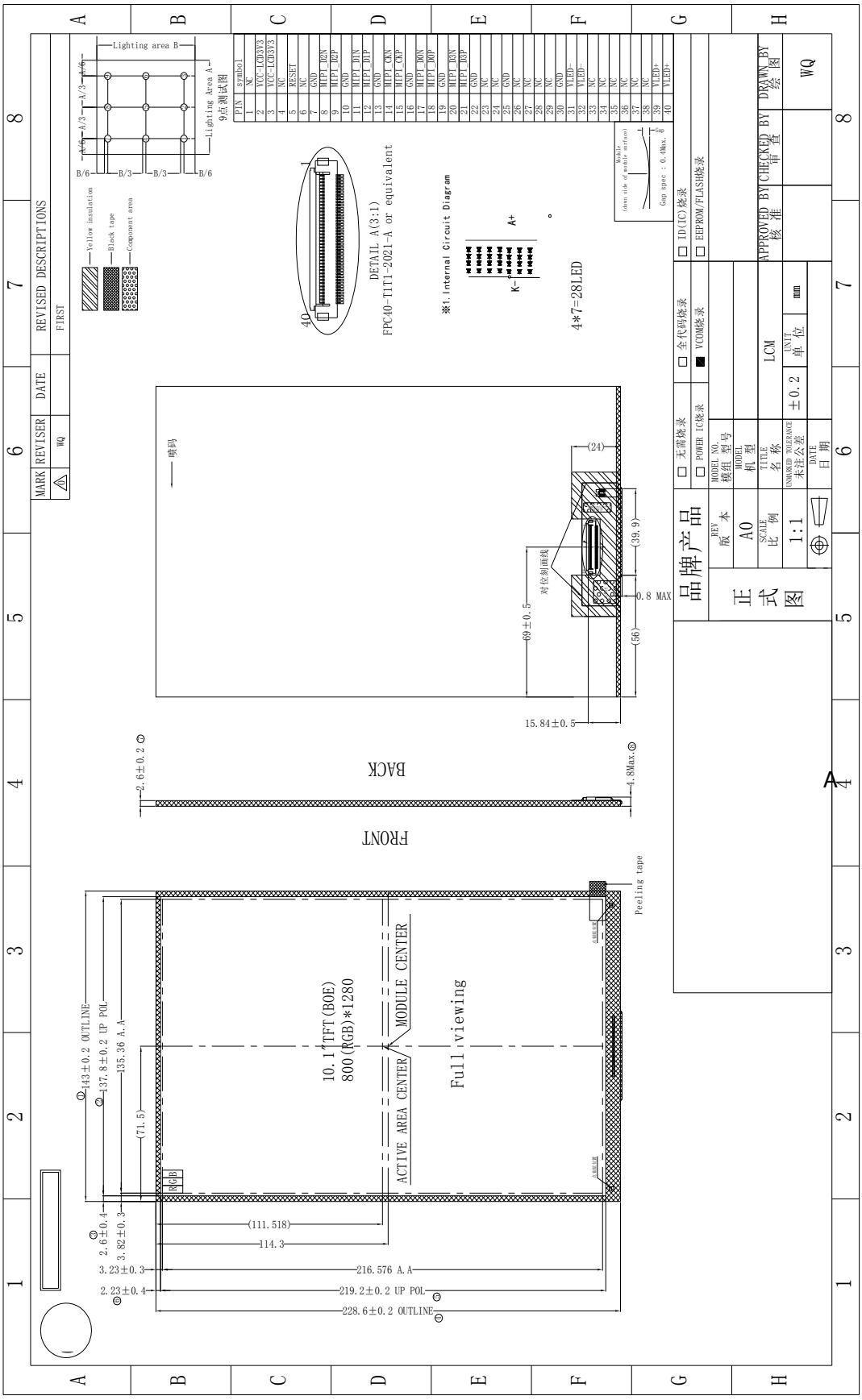
1.1 DESCRIPTION

This LCM is a color active matrix thin film transistor (TFT) IPS liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, Driver IC,FPC and Backlight, This TFT LCD has a 10.1-inch diagonally measured active display area with WXVGA resolution (800 horizontal by 1280vertical pixel array).

1.2 FEATURES:

No.	Item	Specification	Unit
1	Panel Size	10.1”	inch
2	Number of Pixels	800×RGB (3)×1280	pixels
3	Active Area	135.36(H)x 216.576(V)	mm
4	Pixel Pitch	0.1692(H)×0.1692(V) x RGB	mm
5	Outline Dimension	143(W)×228.6(H)×2.6(D)	mm
6	Number of Colors	16.7M	-
7	Display Mode	Transmission mode, normally black	-
8	Viewing Direction	Full viewing	-
9	Display Format	RGB vertical stripe	-
10	Surface Treatment	Anti Glare	-
11	Interface	MIPI	-
12	Backlight	White LED	-
13	Weight	TBD	g

2. MECHANICAL SPECIFICATION



3. PIN DESCRIPTION

FPC Connector FPC is used for the module electronics interface.

No.	Symbol	Function	Remark
1	NC	No connection	
2	VDDLCD3V3	power Voltage for digital circuit	
3	VDDLCD3V3	power Voltage for digital circuit	
4	NC	No connection	
5	RESET	Global reset pin(1.8V)	
6	NC	No connection	
7	GND	Ground	
8	MIPI_D2N	Negative MIPI differential data input	
9	MIPI_D2P	Positive MIPI differential data input	
10	GND	Ground	
11	MIPI_D1N	Negative MIPI differential data input	
12	MIPI_D1P	Positive MIPI differential data input	
13	GND	Ground	
14	MIPI_CKN	Negative MIPI differential clock input	
15	MIPI_CKP	Positive MIPI differential clock input	
16	GND	Ground	
17	MIPI_D0N	Negative MIPI differential data input	
18	MIPI_D0P	Positive MIPI differential data input	
19	GND	Ground	
20	MIPI_D3N	Negative MIPI differential data input	
21	MIPI_D3P	Positive MIPI differential data input	
22	GND	Ground	
23	NC	No connection	
24	NC	No connection	
25	GND	Ground	
26	NC	No connection	
27	NC	No connection	
28	NC	No connection	
29	NC	No connection	
30	GND	Ground	
31	VLED-	LED Cathode	
32	VLED-	LED Cathode	

33	NC	No connection	
34	NC	No connection	
35	NC	No connection	
36	NC	No connection	
37	NC	No connection	
38	NC	No connection	
39	VLED+	LED Anode	
40	VLED+	LED Anode	

4. ELECTRICAL CHARACTERISTICS

4.1 ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Min.	Max.	Unit
Digital Supply Voltage	VDD	-0.3	4.0	V

4.2 TFT LCD MODULE

4.2.1 OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit
Digital Power Supply Voltage	VDD	3.0	3.3	3.6	V

4.3 CURRENT CONSUMPTION

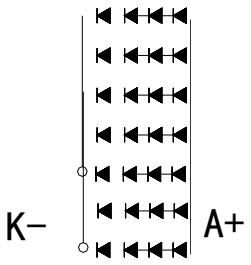
Item	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
Digital Current	IVDD	VDD = 3.3V	-	TBD	-	mA
LCM Power Consumption	PC		-	TBD	-	mW

4.4 BACK LIGHT UNIT

Ta=25℃

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LED current	ILED		140		mA	Total LED
Forward voltage	VF	-	12	-	V	IF=140mA

※1. Internal Circuit Diagram

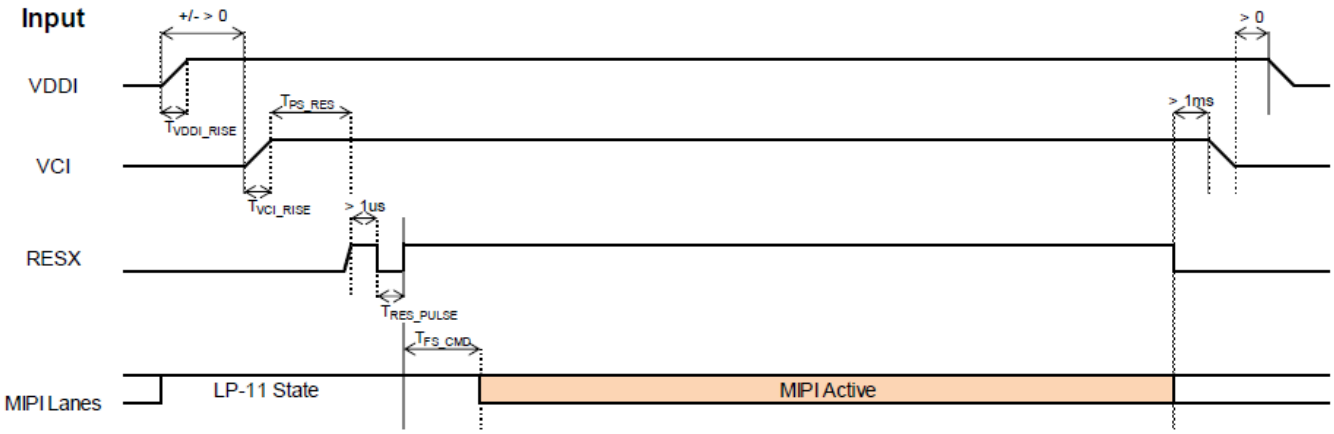


4*7=28LED

4.5 POWER ON/OFF SEQUENCE

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications.

POWER ON/OFF:



Symbol	Characteristics	Min.	Typ.	Max.	Units
T_{VDDI_RISE}	VDDI Rise time	20	-	-	us
T_{VCI_RISE}	Case A: VCI Rise time	200	-	-	us
T_{PS_RES}	VDDI/VCI on to Reset high	10	-	-	ms
T_{RES_PULSE}	Reset low pulse time	10	-	-	us
T_{FS_CMD}	Reset to first command	10	-	-	ms

5. INPUT SIGNAL TIMING

5.1 DC Characteristics for DSI LP Mode

DC levels of the LP-00, LP-01, LP-10 and LP-11 are defined in the table below: DC Characteristics for the DSI LP mode when LP-RX, LP-CD or LP-TX is mentioned in the condition column. Other logical levels in the table are for MCU interface.

Parameter	Symbol	Condition	Specification			Unit
			Min.	Typ.	Max.	
Logic 1 input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic 0 input voltage	V_{ILLPCD}	LP-CD	0.0	-	200	mV
Logic 1 input voltage	V_{IHLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	880	-	1350	mV
Logic 0 input voltage	V_{ILLPRX}	LP-RX (CLK, D0 ,D1, D2, D3)	0.0	-	550	mV
Logic 0 input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0.0	-	300	mV
Logic 1 output voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic 0 output voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic 1 input current	I_{IH}	LP-CD, LP-RX	-	-	10	uA
Logic 0 input current	I_{IL}	LP-CD, LP-RX	-10	-	-	uA

Notes:

1.Ta = -30℃ to 70℃ (to +85℃ no damage)

2. DSI High Speed mode is off.

DC Characteristics for DSI HS mode

Parameter	Symbol	Condition	Specification			Unit
Input Common Mode Voltage for Clock	V_{CMCLK}	CLKP/N Note 2, Note 3	70	-	330	mV
Input Common Mode Voltage for Data	V_{CMDATA}	DnP/N Note 2, Note 3, Note 5	70	-	330	mV
Common Mode Ripple for Clock Equal or Less than 450MHz	$V_{CMRCLKL450}$	CLKP/N Note 4	-50	-	50	mV
Common Mode Ripple for Data Equal or Less than 450MHz	$V_{CMRDATAL450}$	DnP/N Note 4, Note 5	-50	-	50	mV
Common Mode Ripple for Clock More than 450MHz (peak sine wave)	$V_{CMRCLKM450}$	CLKP/N	-	-	100	mV
Common Mode Ripple for Data More than 450MHz (peak sine wave)	$V_{CMRDATAM450}$	DnP/N Note 5	-	-	100	mV
Differential Input Low Level Threshold Voltage for Clock	$V_{THLCLK-}$	CLKP/N	-70	-	-	mV
Differential Input Low Level Threshold Voltage for Data	$V_{THLDATA-}$	DnP/N Note 5	-70	-	-	mV
Differential Input High Level Threshold Voltage for Clock	$V_{THHCLK+}$	CLKP/N	-	-	70	mV
Differential Input High Level Threshold Voltage for Data	$V_{THHDATA+}$	DnP/N Note 5	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	CLKP/N, DnP/N Note 3, Note 5	-40	-	-	mV
Single-ended Input High Voltage	V_{IHHS}	CLKP/N, DnP/N Note 3, Note 5	-	-	460	mV
Differential Termination Resistor	R_{TERM}	CLKP/N, DnP/N Note 5	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	CLKP/N, DnP/N Note 5	-	-	450	mV
Termination Capacitor	C_{TERM}	CLKP/N, DnP/N Note 5, Note 6	-	-	60	pF

Notes:

1. Ta = -30℃ to 70℃ (to +85℃ no damage) , VCI = 2.5V to 6.0V, VDDI = 1.65V to 3.3V

2. Includes 50mV (-50mV to 50mV) ground difference

3. Without VCMRCLKM450/VCMRDATAM450

4. Without 50mV (-50mV to 50mV) ground difference

5. n = 0 and 1

6. For higher bit rates, a 14pF capacitor will be needed to meet the common-mode return loss specification.

5.2 AC CHARACTERISTICS

High Speed Mode – Clock Channel Timing

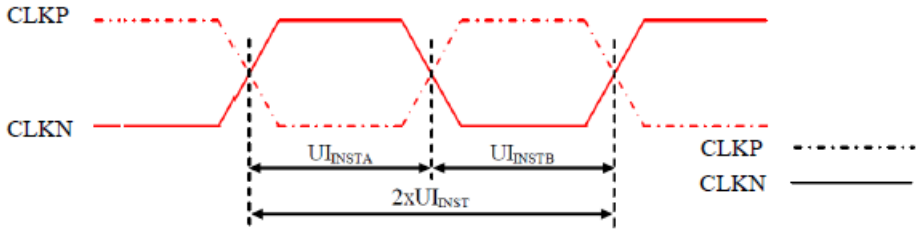


Figure 117: DSI Clock Channel Timing

Table 38: DSI Clock Channel Timing

Signal	Symbol	Parameter	Min	Max	Unit
CLKP/N	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
CLKP/N	UI_{INSTA},UI_{INSTB} (Note 1)	UI instantaneous Half	2 (Note 2)	12.5	ns

Notes:

1. UI = UIINSTA = UIINSTB

2. Define the minimum value of 24 UI per Pixel, see Table 39.

Table 39: Limited Clock Channel Speed

Data type	Two Lanes speed	Three Lanes speed	Four Lanes speed
Data Type = 00 1110 (0Eh), RGB 565, 16 UI per Pixel	566 Mbps	433 Mbps	366 Mbps
Data Type = 01 1110 (1Eh), RGB 666, 18 UI per Pixel	637 Mbps	487 Mbps	412 Mbps
Data Type = 10 1110 (2Eh), RGB 666 Loosely, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps
Data Type = 11 1110 (3Eh), RGB 888, 24 UI per Pixel	850 Mbps	650 Mbps	550 Mbps

HIGH SPEED MODE DATA CLOCK CHANNEL TIMING

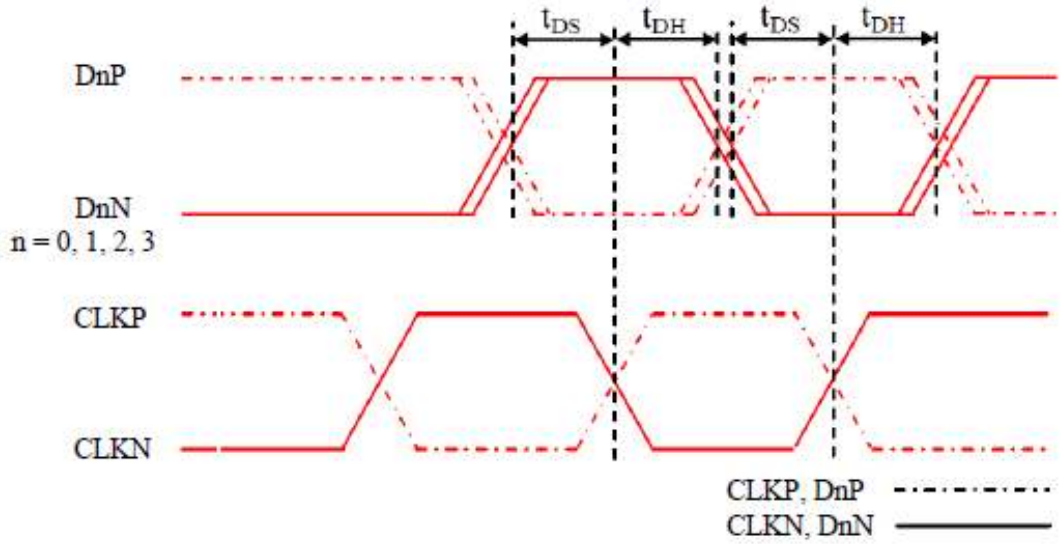


Figure 118: DSI Data to Clock Channel Timings

Table 40: DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DnP/N , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

5.3 PARALLEL RGB INPUT TIMING TABLE

5.3.1 HORIZONTAL VERTICAL TIMING

Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Horizontal Display Area	thd		800		DCLK
DCLK frequency	fclk	63.06	67.28	81.51	MHz
HS pulse width	thpw	-	20	-	DCLK
Hs Back Porch(Blanking)	thd		20		DCLK
Hs Front Porch	thfp	-	20	-	DCLK

Vertical Timing

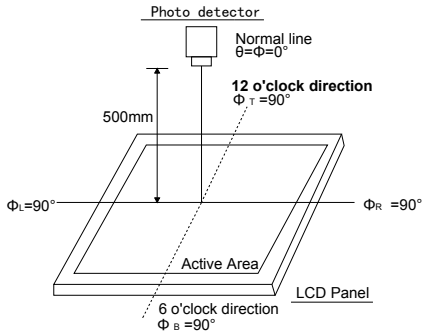
Parameter	Symbol	Spec.			Unit
		Min.	Typ.	Max.	
Vertical Display Area	tvd		1280		TH
VS Pulse Width	tvpw	-	4	-	TH
VS Back Porch(Blanking)	tvb		4		TH
VS Front Porch	tvfp	-	16	-	TH

6. OPTICAL CHARACTERISTICS

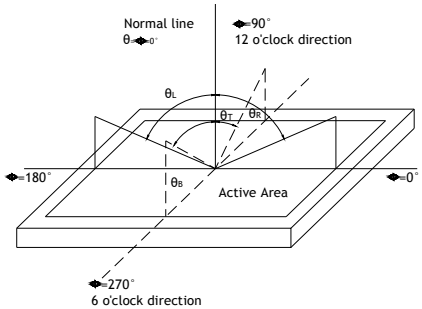
Ta=25±2℃

Item		Symbol	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR-					Note1 Note3
Luminance(center)		L	280	300	-	cd/m2	Note1 Note5 Note7
Luminance uniformity		YU	80	90		%	Note7
Response Time		Rising + Falling	-	30	35	ms	Note1 Note4
Viewing Angle K=Contrast Ratio>10	Horizontal	θx^+	80	85	-	degree	Note2
		θx^-	80	85	-		
	Vertical	θy^+	80	85	-		
		θy^-	80	85	-		
Color Chromaticity (CIE1931)	Red	x	Typ-0.05	0.610	Typ+0.05		Note1 Note5 Note7
		y		0.370			
	Green	x		0.320			
		y		0.590			
	Blue	x		0.180			
		y		0.120			
	White	x		0.310			
		y		0.330			
Colorgamut(NTSC ratio)				53		%	

Note1: Definition of optical measurement system (BM-7)



Note2: Definition of viewing angle range and measurement system
Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80).



Note3: Definition of Response time

The response time is defined as the LCD optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector outputintensity changed from 90% to 10%. And fall time (TOFF) is the time between photodetector output intensity changed from 10% to 90%.

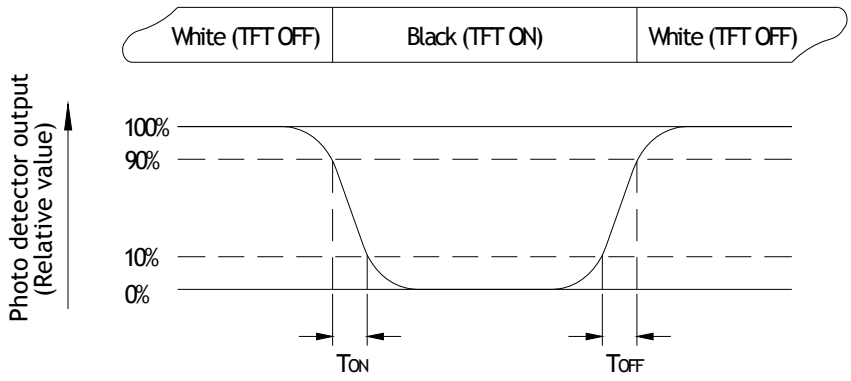


Fig. 6-3 Definition of response time

Note4: Definition of contrast ratio

$$\text{Contrast ratio(CR)}=\frac{\text{Luminance measured when LCD on the Whitestate}}{\text{Luminance measured when LCD on the Blackstate}}$$

"White state ": The state is that the LCD should drive by Vwhite.

"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

Note5: Definition of color chromaticity (CIE1931)

Color coordinates measured at center point of LCD.

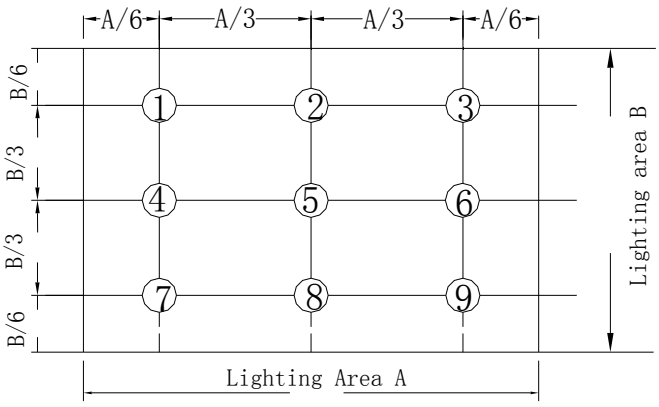
Note6: All input terminals LCD panel must be ground while measuring the center area of the panel. The LED driving condition is IL=

140mA Note7: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas.Everymeasuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L----Active area length, W---- Active area width



Bmax: The measured maximum luminance of all measurement position.

Bmin: The measured minimum luminance of all measurement position.

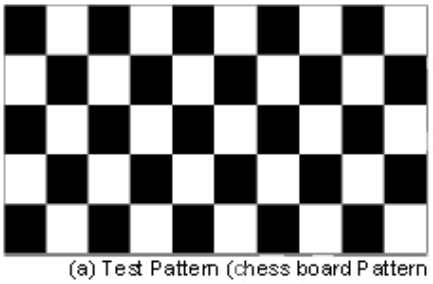
7. RELIABILITY TEST ITEMS

7.1 TEMPERATURE AND HUMIDITY

Test Item	Test Condition	Remark
HighTemperatureStorage	Ta=60℃; 48hrs	
Low Temperature Storage	Ta=-20℃;48hrs	
High Temperature Operation	Ta=50℃，48Hrs	
LowTemperatureOperation	Ta=-10℃; 48hrs	
HighTemperatureHighHumidity Operation	Ta=60℃，90%RH，72Hrs(no condensation)	
Thermal Shock	-10℃(0.5h) ~ 60℃(0.5h) / 50 cycles	
Image Sticking	25℃ ; 1hrs	

Note1:Condition of image sticking test :25℃±2℃

Operation with test pattern sustained for 1hrs,then change to 50% gray pattern immediately. after 5 mins, the mura must be disappeared completely



(a) Test Pattern (chess board Pattern)

(b) Gray Pattern

7.2 VIBRATION & SHOCK

Test item	Conditions	Remark
Packing Shock (non-operation)	980m/s2,6ms, ±x,y,z 3times for direction	
Packing Vibration (non-operation)	Frequency range:10 HZ~50HZ Stroke:1.0mm,sweep:10 HZ ~50HZ x,y,z 2 hours for each direction	

7.3ESD

Test item	Conditions	Remark	
Electro Static Discharge Test (non-operation)	150pF，330Ω，Contact:±4KV,Air:±8KV	1	Class C
	200pF，0Ω，±200V contact test	2	

Note: Measure point :

1. LCD glass and metal bezel
2. IF connector pins

8. GENERAL PRECAUTION

8.1 SAFETY

1. Do not swallow any liquid crystal, even if there is no proof that liquid crystal ispoisonous.
2. If the LCD panel breaks, be careful not to get liquid crystal to touch your skin.
3. If skin is exposed to liquid crystal, wash the area thoroughly with alcohol or soap.

8.2 STORAGE CONDITIONS

1. Store the panel or module in a dark place where the temperature is 23±5°C andThehumidity is below 50±20%RH.
2. Store in anti-static electricity container.
3. Store in clean environment, free from dust, active gas, and solvent.
4. Do not place the module near organics solvents or corrosive gases.
5. Do not crush, shake, or jolt the module.

8.3 HANDLING PRECAUTIONS

1. Avoid static electricity which can damage the CMOS LSI.
2. The polarizing plate of the display is very fragile. So, please handle it verycarefully.
3. Do not give external shock.
4. Do not apply excessive force on the surface.
5. Do not wipe the polarizing plate with a dry cloth, as it may easily scratch theSurface of plate.
6. Do not use ketonics solvent & Aromatic solvent, use with a soft cloth soaked witha cleaning naphtha solvent.
7. Do not operate it above the absolute maximum rating.
8. Do not remove the panel or frame from the module.
9. When the module is assembled, it should be attached to the system firmly,Be careful not to twist and bend the module.
10. Wipe off water droplets or oil immediately. If you leave the droplets for a long time,staining and discoloration may occur.
11. If the liquid crystal material leaks from the panel, it should be kept away from the eyesormouth in case of contact with hands, legs or clothes, it must be washedawaythoroughly with soap.

8.4 WARRANTY

1.The period is within twelve months since the date of shipping out under normal using and storage conditions.
2. Do not repaired or modified the LCM. It may cause function to lose efficacy,Starry does not warrant the LCM.
3. All process and material comply ROHS.

9. PACKAGE DRAWING