SPECIFICATION

FOR

TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HL MODEL : HG101WQ004T01

□**Preliminary Specification**

■**Final Specification**

Customer Confirmation column:

Approved by :_____Dept. :_____Data :_____

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

Designed by	Checked by	Approved by

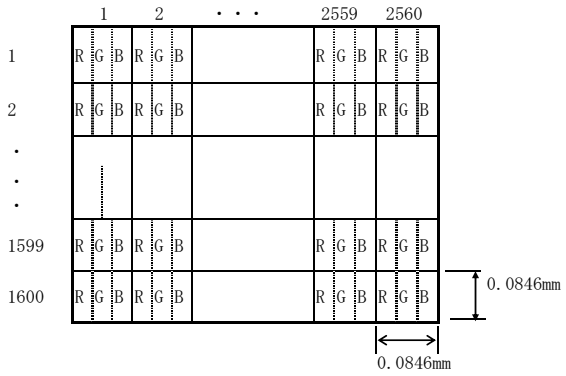
1.BASIC SPECIFICATIONS

1.1 STRUCTURES

HG101WQ004T01is 10.1" color TFT -LCD (Thin Film Transistor Liquid Crystal Display) module composed of LCD panel , driver ICs ,control circuit, Utilizes a panel with a 16:10 aspect ratio. The 10.1"screen produces a high resolution image that is composed of 2560x1600 pixel elements in a stripe arrangement.

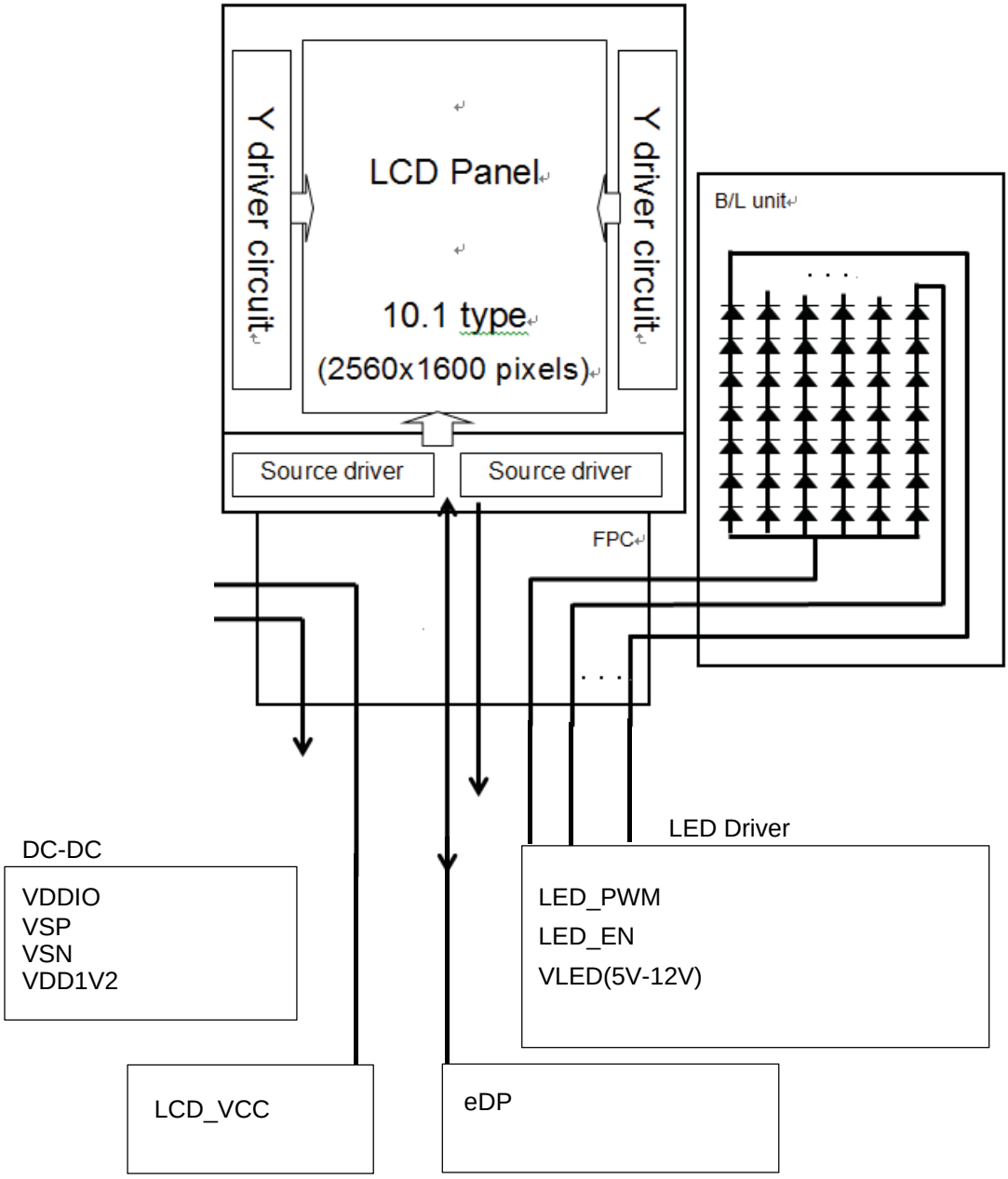
General specifications are summarized in the following table:

		Spec
General	LCD type	IPS
	Diagonal size	**10.1" Landscape**
	Resolution	**WQXGA (2560xRGBx1600)**
	Active area	216.576 mm(H) x 135.36 mm(V)
	Pixel Pitch	28.2 um(H) x 84.6um(V)
	PPI	300
	Panel Type	LTPS
Interface	Interface	4lane eDP 1.3
Optical	Luminance	Typ.400 cd/m2 @20mA
	Color gamut	Typ. 77.1% (NTSC) 108.8% (sRGB)
	Contrast	Typ.1000:1
	Number of colors	16M (24bit)
	Viewing angle	L/R/T/B > 80 @CR>10
Back Light	Number of LEDs	48
	LED current	20mA
LCD Panel	Glass size	220.58 mm(H) x 143.76 mm(V) x 0.36mm
	Glass border(L/R/T/B)	2.0/2.0/2.0/6.4
	Glass Thickness	0.36mm(0.18+0.18)
Module	Module structure	LCD panel + FPC + BL
	Module border (L/R/T/B)	2.502 / 2.502 / 2.5 / 6.9
	Module/TP dimensions	225.25 mm(H) x 149.05 mm(V) x 3.74 mm(D) ※ w/o FPC & CG



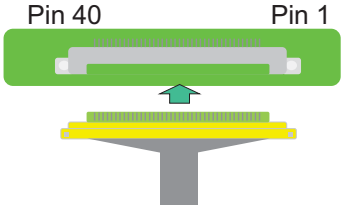
The LCD Products listed on this document are not suitable for use of aerospace equipments, submarine cables, nuclear reactor control systems and life support systems. If customers intend to use these LCD products for above applications or not listed in "Standard" as follows, please contact our sales people in advance.

1.2 BLOCK DIAGRAM



1.3 INTERFACE PINS

CONNECTOR (MSAK24025P40)

Pin	Symbol	Description	Notes
1	NC Reserved	Reserved for LCD manufacturer's use	
2	GND	High Speed Ground	
3	Lane3_N	Complement Signal Link Lane 3	
4	Lane3_P	True Signal Link Lane 3	
5	GND	High Speed Ground	
6	Lane2_N	Complement Signal Link Lane 2	
7	Lane2_P	True Signal Link Lane 2	
8	GND	High Speed Ground	
9	Lane1_N	Complement Signal Link Lane 1	
10	Lane1_P	True Signal Link Lane 1	
11	GND	High Speed Ground	
12	Lane0_N	Complement Signal Link Lane 0	[Connector] MSAK24025P40 (40pin , 0.5pitch)
13	Lane0_P	True Signal Link Lane 0	
14	GND	High Speed Ground	
15	AUX_CH_P	True Signal Auxiliary Channel	
16	AUX_CH_N	Complement Signal Auxiliary Channel	
17	GND	High Speed Ground	
18	VCC	LCD logic and driver power	[Connector pin arrangement] Pin 40 Pin 1 
19	VCC	LCD logic and driver power	
20	VCC	LCD logic and driver power	
21	VCC	LCD logic and driver power	
22	NC Reserved	Reserved for LCD manufacture's use	
23	GND	LCD logic and driver ground	
24	GND	LCD logic and driver ground	
25	GND	LCD logic and driver ground	
26	GND	LCD logic and driver ground	
27	HPD	HPD signal pin	
28	BL_GND	LED Backlight ground	
29	BL_GND	LED Backlight ground	
30	BL_GND	LED Backlight ground	
31	BL_GND	LED Backlight ground	
32	BL ENABLE	LED Backlight control on/off control	
33	BL PWM	System PWM signal input for dimming	
34	NC Reserved	Reserved for LCD manufacture's use	
35	NC Reserved	Reserved for LCD manufacture's use	
36	VLED	LED Backlight power (5-12V Typical)	
37	VLED	LED Backlight power (5-12V Typical)	
38	VLED	LED Backlight power (5-12V Typical)	
39	VLED	LED Backlight power (5-12V Typical)	
40	NC Reserved	Reserved for LCD manufacture's use	

2. FUNCTIONS

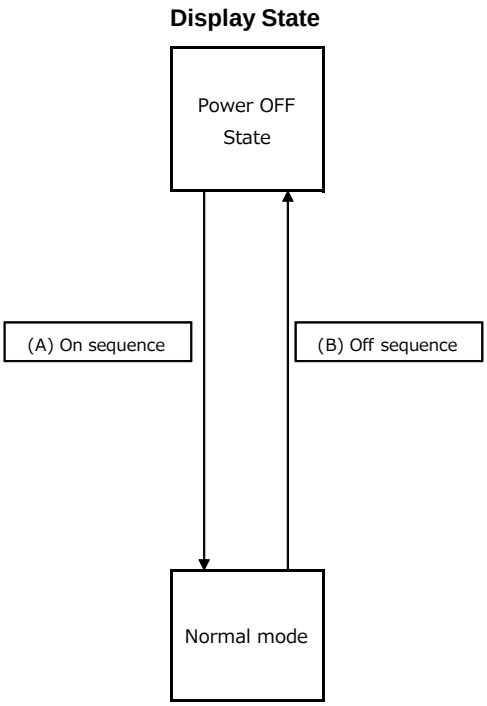
The use of 10.1" WQXGA LCD basically conforms to specifications of LCD driver IC (Renesas SP).

It explains typical function in this manual.

2.1 OVERVIEW

The basic operation mode of this LCD module is illustrated below.

When changing from one mode to another, make sure to follow the sequence indicated in the figure.



2.2 INTERFACE

4Lane eDP to MIPI Video mode 4 Data Lanesand 2 clock lane with 2ports

HS(High Speed) Transmission (Unidirectional)

LP(Low Power) Transmission (Bidirectional)

Diagnostic function - checksum and ECC error monitoring

Functionality supported by Escape mode

Clock Lane supports ULPS

Packet - Based Protocol

3. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit	Remarks
power supply voltage	LCD_VCC	-0.3~4.6	V	LCD_VCC-GND
LED Enable Input	VLED_EN	-0.3~27	V	VLED_EN-GND
PWM EN demming range	FPWM	-	Hz	IOVCC-GND
operating temperature range (environmental)	TOP	0 to 50	℃	no dew condition
storage temperature range (environmental)	TST	-20 to 60	℃	no dew condition

Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

4. ELECTRICAL SPECIFICATIONS

4.1 DC SPECIFICATIONS

4.1.1 DC specifications of general pins

GND = 0V, Ambient temperature = 25°C

Parameter	Symbol	Condition	Ratings			Unit	Pins
			Min.	Typ.	Max.		
Power supply voltage	LCD_VCC		3.2	3.3	3.4	V	
Low-level input voltage	VIL		0	-	0.3 x IOVCC	V	
High-level input voltage	VIH		0.7 x IOVCC	-	IOVCC	V	
Low-level output voltage	VOL	IOUT=+1mA	0.0	-	0.2 x IOVCC	V	
High-level output voltage	VOH	IOUT=-1mA	0.8 x IOVCC	-	IOVCC	V	
Power supply current(DC-DC)	IVCC		-	480	-	mA	LCD_VCC

*1: Rated values indicate operating range of electrical functions.

*2: When it is the power supply voltage Typ.

*3: Display image is “White raster Display shown in describes..

<White raster Display>

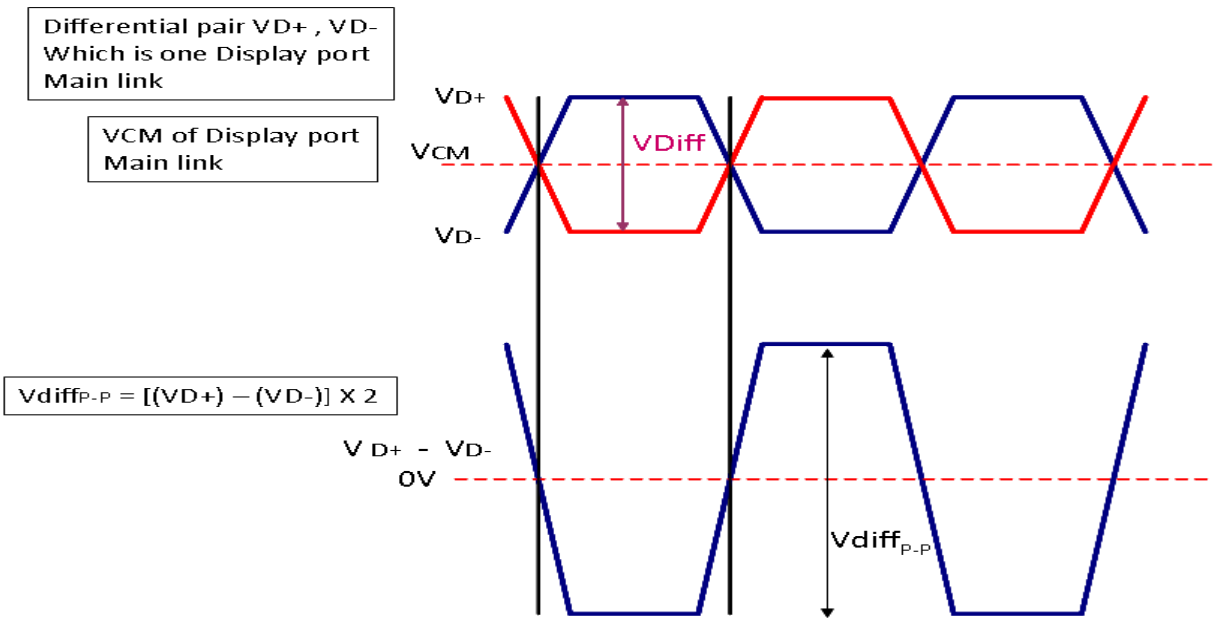
ELECTRICAL CHARACTERISTICS

Ta=25℃

ITEM	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
LED Total Iuput Voltage	VLED	5	12	24	V	
LED Total Input Current	IBL+	-	120	-	mA	
LED Enable Input	VLED_EN	2.7	-	5.5	V	
Duty cycle range	PWM	100	-	30K	Hz	

4.2 Signal Electrical Characteristics

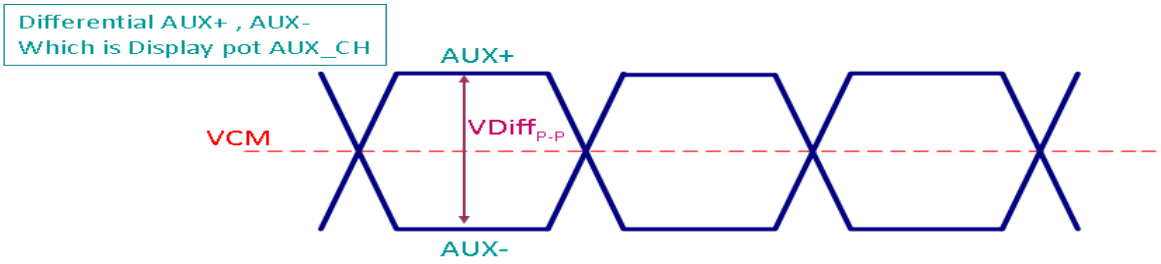
4.2.1 Display Port main link signal:



Display port main link					
		Min	Typ	Max	unit
VCM	RX input DC Common Mode Voltage		0		V
$VDiff_{P-P}$	Peak-to-peak Voltage at a receiving Device	100		1320	mV

Fallow as VESA display port standard V1.1a

4.2.2 Display Port AUX_CH signal:



Display port AUX_CH					
		Min	Typ	Max	unit
VCM	AUX DC Common Mode Voltage		0		V
$VDiff_{P-P}$	AUX Peak-to-peak Voltage at a receiving Device	0.4	0.6	0.8	V

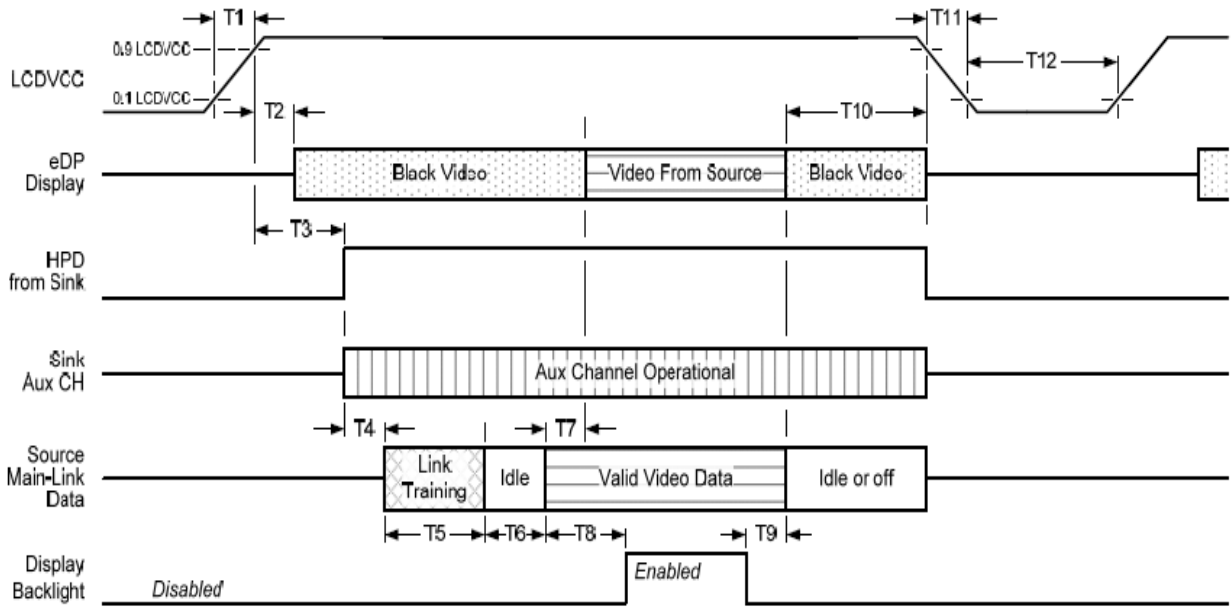
Fallow as VESA display port standard V1.1a.

4.2.2 Display Port VHPD signal:

Display port VHPD					
		Min	Typ	Max	unit
VHPD	HPD Voltage	2.25		3.6	V

4.3 RECOMMENDED SEQUENCE

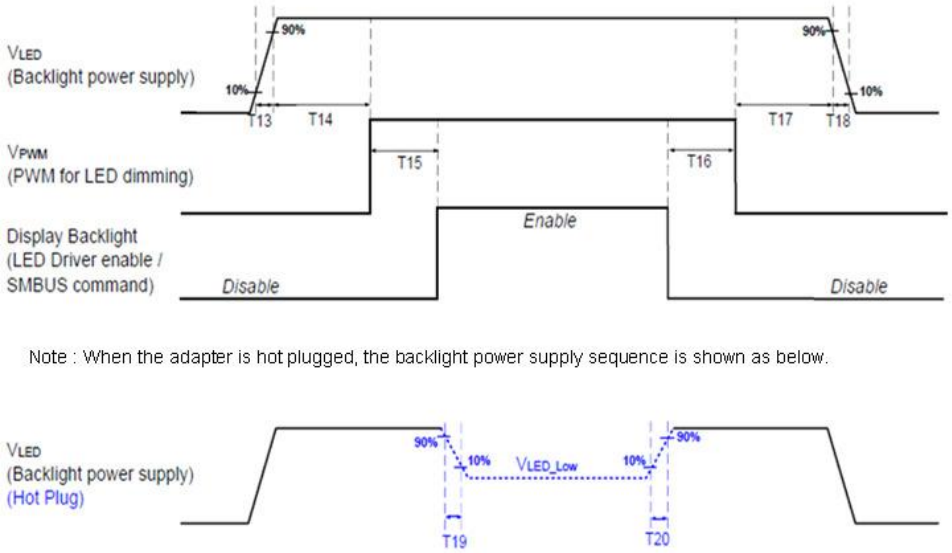
4.3.1 Display Port panel power sequence:



4.3.2 Display Port panel power sequence timing parameter:

Timing parameter	Description	Reqd. by	Limits			Notes
			Min.	Typ.	Max.	
T1	power rail rise time, 10% to 90%	source	0.5ms		10ms	
T2	delay from LCDVDD to black video generation	sink	0ms		200ms	prevents display noise until valid video data is received from the source
T3	delay from LCDVDD to HPD high	sink	122ms		200ms	sink AUX_CH must be operational upon HPD high.
T4	delay from HPD high to link training initialization	source				allows for source to read link capability and initialize.
T5	link training duration	source				dependant on source link to read training protocol
T6	link idle	source				Min accounts for required BS-Idle pattern. Max allows for source frame synchronization.
T7	delay from valid video data from source to video on display	sink	0ms		50ms	max allows sink validate video data and timing.
T8	delay from valid video data from source to backlight enable	source				source must assure display video is stable.
T9	delay from backlight disable to end of valid video data	source				source must assure backlight is no longer illuminated.
T10	delay from end of valid video data from source to power off	source	0ms		500ms	
T11	power rail fall time, 90% to 10%	source			10ms	
T12	power off time	source	500ms			

4.3.3 Display Port panel power sequence timing parameter:



	Min (ms)	Max (ms)
T13	0.5	10
T14	10	-
T15	10	-
T16	10	-
T17	10	-
T18	0.5	10
T19	1*	-
T20	1*	-

Seamless change: T19/T20 = 5xT_{PWM}*

*T_{PWM}= 1/PWM Frequency

Note : When the adapter is hot plugged, the backlight power supply sequence is shown as below.

4.3.4 Timing Chart

Basically, interface timings should match the 2560x1600 /60Hz manufacturing guide line timing.

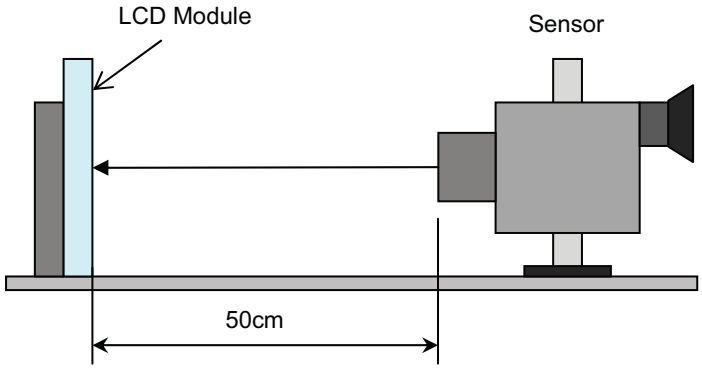
Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		---	--	60	---	Hz
Clock frequency		1/ T_{Clock}	259.7	269.0	315.3	MHz
Vertical Section	Period	T_V	1640	1649	1800	T_{Line}
	Active	T_{VD}	1600			
	Blanking	T_{VB}	40	49	200	
Horizontal Section	Period	T_H	2640	2720	2920	T_{Clock}
	Active	T_{HD}	2560			
	Blanking	T_{HB}	80	160	200	

Note1 : DE mode only

5. OPTICAL CHARACTERISTICS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Notes
Brightness		B	φ=0°, θ=0°	350	(400)	-	Cd/m2	(1),(2)
Viewing Angle on axis	φ=0	θ	CR>10	(80)	-	-	degree	(3),(4)
	φ=90							
	φ=180							
	φ=270							
Contrast Ratio		CR	φ=0°, θ=0°	-	(1200)	-	-	(5)
Color Gamut CIE 1931 (Primary Color)	Red	x	φ=0°, θ=0°	-	0.6379	-	-	-
		y		-	0.3393	-		
	Green	x		-	0.3179	-		
		y		-	0.647	-		
	Blue	x		-	0.1502	-		
		y		-	0.0461	-		
	White	x		-	0.2911	-		
		y		-	0.3082	-		
NTSC Ratio (CIE1931)		-	φ=0°, θ=0°	-	(77)	-	-	
Gamma Curve		-	φ=0°, θ=0°	-	(2.2)	-	-	
Cross Talk		CT	-	-	-	(4)	%	(6)

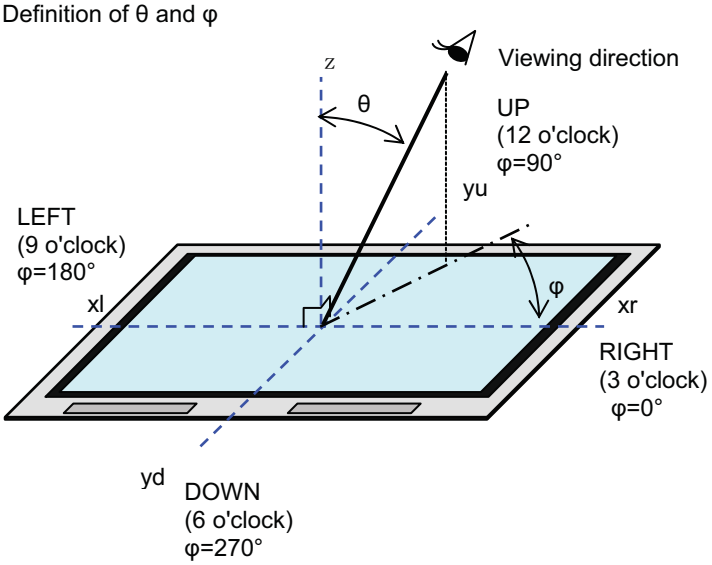
Notes (1) Definition of Brightness "B". At the Center of Active Area.



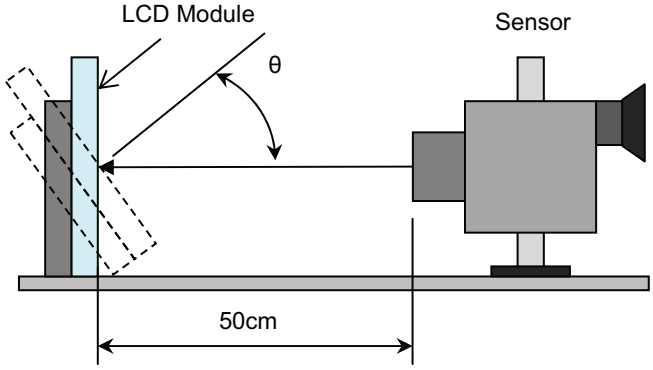
Sensor : KONICA MINOLTA CS-1000 or equivalent

(2) Display image for measurement : All White

(3) Definition of θ and φ



(4) Definition of Viewing Angle θ



Sensor : TOPCON's BM-5A or equivalent

(5) Definition of Contrast "CR"

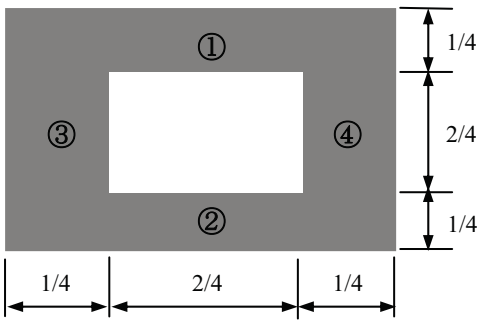
CR = (Brightness when displaying White raster) / (Brightness when displaying Black raster)

(6) Definition of Cross Talk "CT"

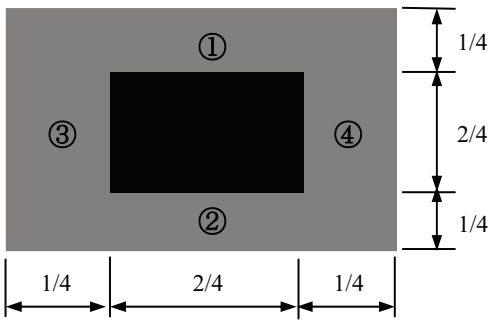
CT = {(Brightness [Cross-talk pattern]) – (Brightness [127Gray])} / (Brightness [127Gray]) x 100(%)

Measurement pattern :
Cross talk pattern 1 : White box
Cross talk pattern 2 : Black box

Measurement Point :
Vertical Crosstalk : ① and ②
Horizontal Crosstalk : ③ and ④



Cross talk pattern 1 : White box



Cross talk pattern 2 : Black box

6. DIMENSIONAL OUTLINE