SPECIFICATION

FOR

TFT LCD MODULE

CUSTOMER : _____

CUSTOMER MODULE : _____

HG MODEL : HG070WS060

☐ **Preliminary Specification**

■ **Final Specification**

Customer Confirmation column:

Approved by :_____ Dept. :_____ Data :_____

Please return one of the copies of the specification with your signature to us within two weeks after you receive this document. If it is not returned, we will assume that you agree to the entire contents of this specification document.

Designed by	Checked by	Approved by

REVISION RECORD

REV NO	REV DATE	CONTENTS	REMARKS
V.0	2025-06-03	First Release	

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1.0 General description

1.1 Introduction

HG070WS060T01 is model a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. This model is composed of a TFT LCD panel, a driving circuit and a back light system. This TFT LCD has a 7.0 inch diagonally measured active display area with WSVGA (1024 horizontal by 600 vertical pixel array) resolution. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.

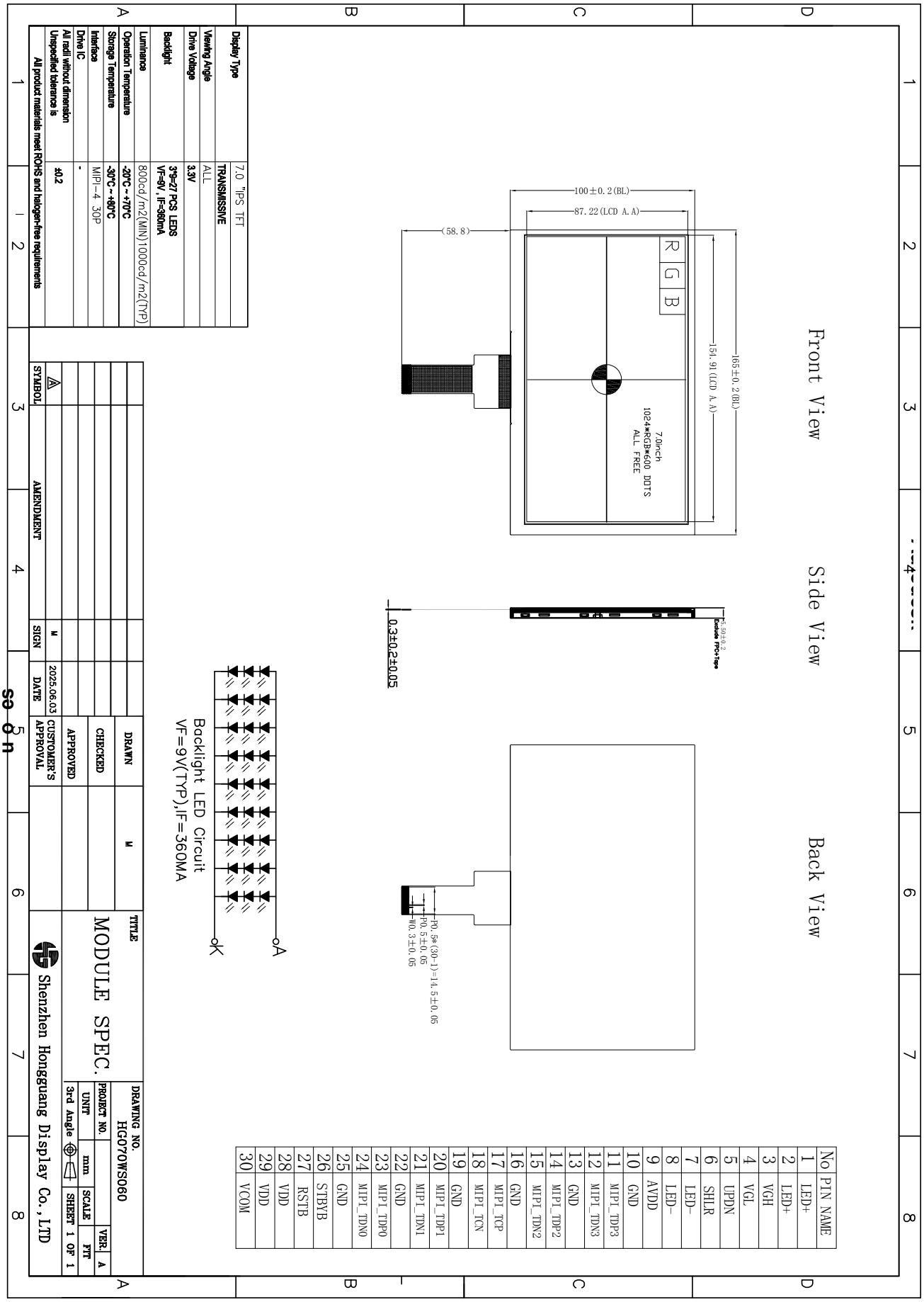
1.2 Features

- **4 lanes MIPI Interface**
- Low driving voltage and low power consumption
- ROHS Compliant

1.3 General information

Item	Dimension	Unit
Size	7.0	inch
Dot Matrix	1024x RGB x 600	dots
Module dimension(FPC not include)	165.00(W) x100.00(H) x 5.50(T)	mm
Active area	154.21(W) x 85.92(H)	mm
Dot pitch	0.0502(H)x0.1432(V)	mm
Brightness (Typ)	1000	cd/m^2
Product type	Normally Black	
Display colors	16.7M	
Viewing Angle	ALL FREE	
Driver IC	TBD	
Interface	MIPI	
Backlight Type	Normally White	
Display Connector	FPC	
FPC Connector	MIPI-4 30Pin	

2.0 OUTLINE DIMENSION



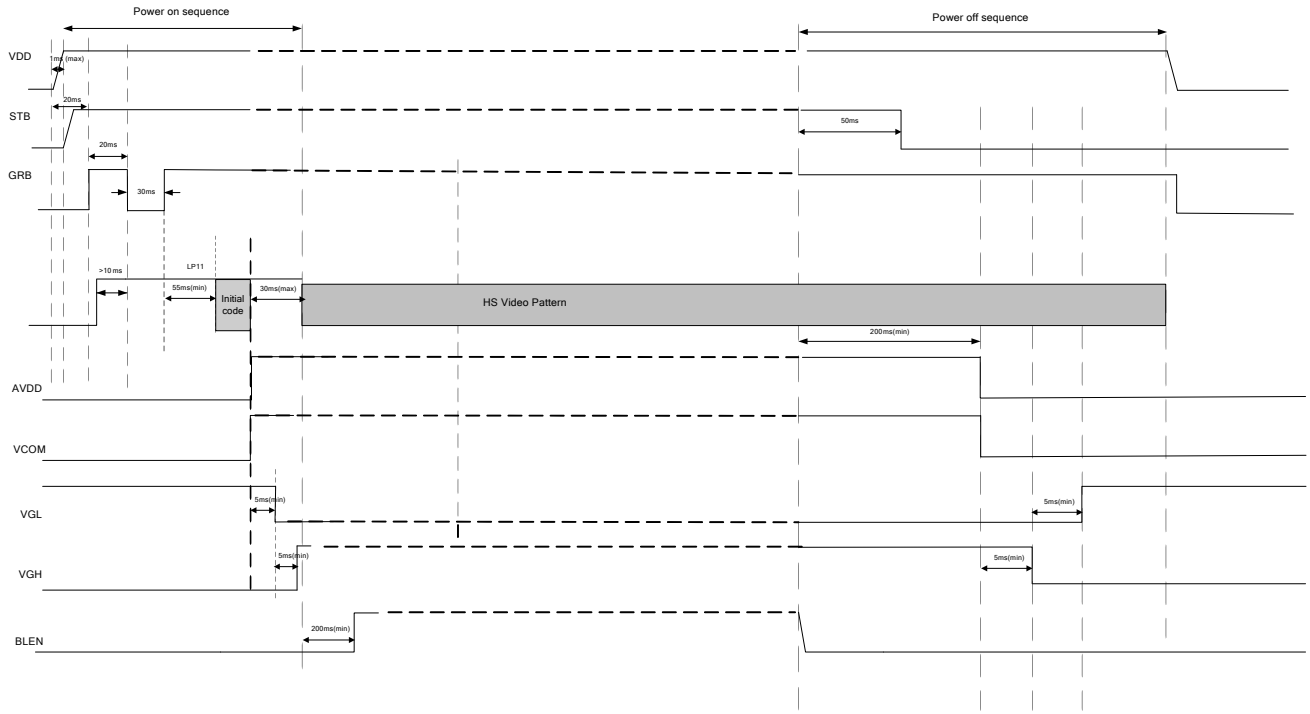
3.0 INTERFACE PIN CONNECTION

3.1 Signal of interface

Terminal No.	Symbol	I/O	Functions
1--2	VLED+	P	Power for LED backlight (Anode)
3	VGH	P	Gate ON Voltage
4	VGL	P	Gate OFF Voltage
5	UPDN	I	Up/down selection
6	SHLR	I	Left / right selection
7--8	VLED-	P	Power for LED backlight (Cathode)
9	AVDD	P	Power for Analog Circuit
10	GND	P	Ground
11	MIPI_D3+	I	Positive MIPI differential data inputs3+
12	MIPI_D3-	I	Negative MIPI differential data inputs3-
13	GND	P	Ground
14	MIPI_D2+	I	Positive MIPI differential data inputs2+
15	MIPI_D2-	I	Negative MIPI differential data inputs2-
16	GND	P	Ground
17	MIPI_CLK+	I	Positive MIPI differential clock inputs+
18	MIPI_CLK-	I	Negative MIPI differential clock inputs-
19	GND	P	Ground
20	MIPI_D1+	I	Positive MIPI differential data inputs1+
21	MIPI_D1-	I	Negative MIPI differential data inputs1-
22	GND	P	Ground
23	MIPI_D0+	I	Positive MIPI differential data inputs0+
24	MIPI_D0-	I	Negative MIPI differential data inputs0-
25	GND	P	Ground
26	STBYB	I	Standby mode, normally pull high STBYB="1", normally operation STBYB="0", timing control, source driver will turn off
27	RESET	P	Global reset pin.
28	DVDD	P	Power for Digital Circuit
29	DVDD	P	Power for Digital Circuit
30	VCOM	P	Common voltage

4.0 Power On/Off Sequence

In order to prevent IC from power on reset fail, the rising time (TPOR) of the digital power supply VDD should be maintained within the given specifications. Refer to “AC Characteristics” for more detail on timing.



Note: CLK and Data Lanes should keep in LP11(stop state) before GRB.

5.0 ELECTRICAL CHARACTERISTICS

5.1 TFT LCD Module

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VDD	1.71	1.8	1.89	V
	VGH	17	18	19	V
	VGL	-7.0	-6.0	-5.0	V
	AVDD	9.2	9.6	10.0	V
VCOM	VCOM	3.0	(3.2)	3.4	V

Note:

(1) VGH is TFT Gate operating voltage.

(2) VGL is TFT Gate operating voltage. The low voltage level of VGH signal must be fluctuates with same phase as Vcom.

5.2 Back-Light Unit

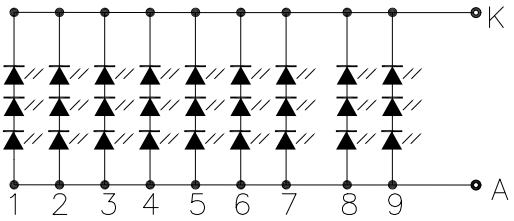
The backlight system is an edge-lighting type with 27 LED.
The characteristics of the LED are shown in the following tables.

Item	Symbol	Min.	Typ.	Max.	Unit	Note
LED current	IL	-	360	-	mA	(2)
LED Voltage	VL	-	9.0	-	V	
Operating LED life time	Hr	20000	-	-	Hour	(1)(2)

Note (1) LED life time (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note (2) The "LED life time" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL=360mA. The LED lifetime could be decreased if operating IL is larger than 360mA. The constant current driving method is suggested.

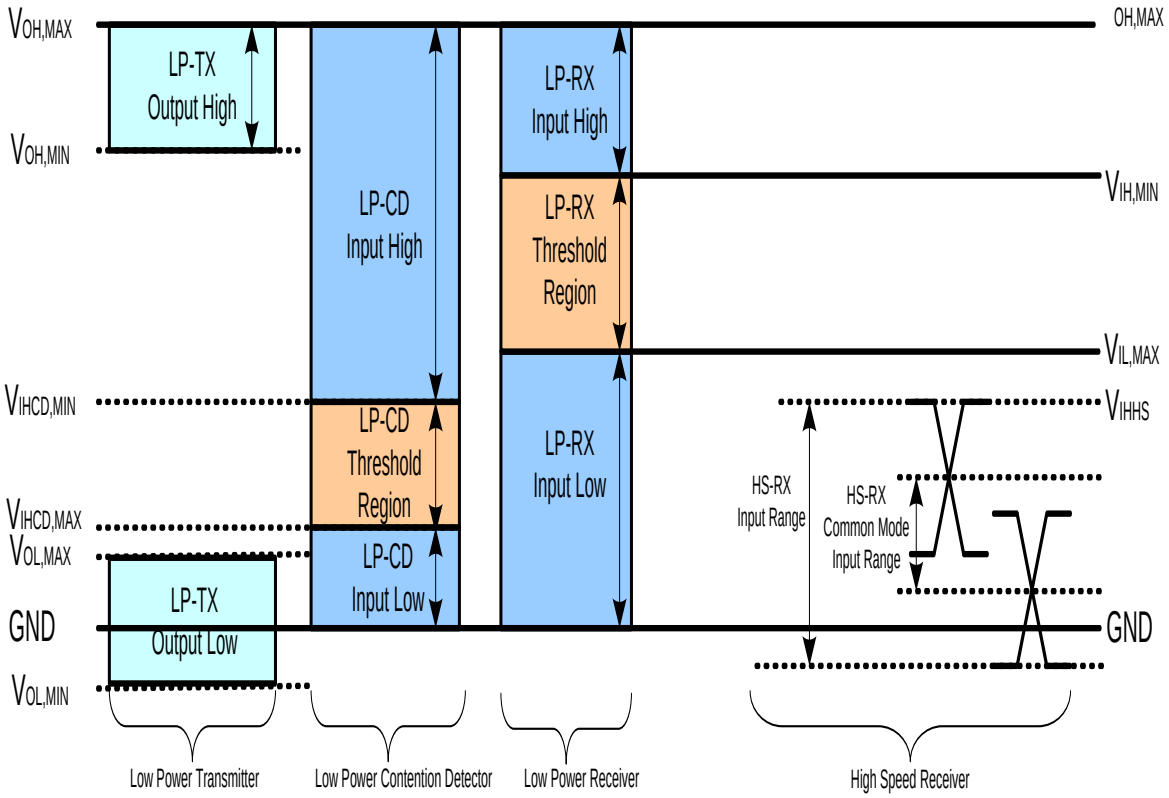
LED CIRCUIT DIAGRAM： 3 x 9 = 27 LED



5.3 DC Characteristics

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Low level input voltage	Vil	For the digital circuit	0	-	0.3×VD	V
High level input voltage	Vih	For the digital circuit	0.7×VDD	-	VDD	V
Input leakage current	Ii	For the digital circuit	-	-	±1	μA
High level output voltage	Voh	Ioh= -400 μA	VDD- 0.4	-	-	V
Low level output voltage	Vol	Iol= +400 μA	-	-	GND+0.	V
Pull low/high resistor	Ri	For the digital input pin @	200K	250	300K	ohm
Digital Operation current	Idd	Fclk=51.2MHz,VDD=VDD_IF=1.8V	-	TB	-	mA
Digital Stand-by current	Ist1	Clock and all functions are stopped	-	10	50	μA
Analog Operating Current	Idda	No load, Fclk=51.2MHz, @AVDD=13.5V,V1=13.4V, V14=0.1V	-	10	12	mA
Logic 0 contention threshold	VILCD,MAX	—	—	200	mV	
Logic 1 contention threshold	VIHCD,MIN	450	—	1350	mV	
Logic high level input current	IIH	—	—	10	uA	
Logic low level input current	IIL	-10	—	—	uA	
Input pulse rejection (DSI-CLKP/N,DSI-DnP/N)	SGD	—	—	300	Vps	



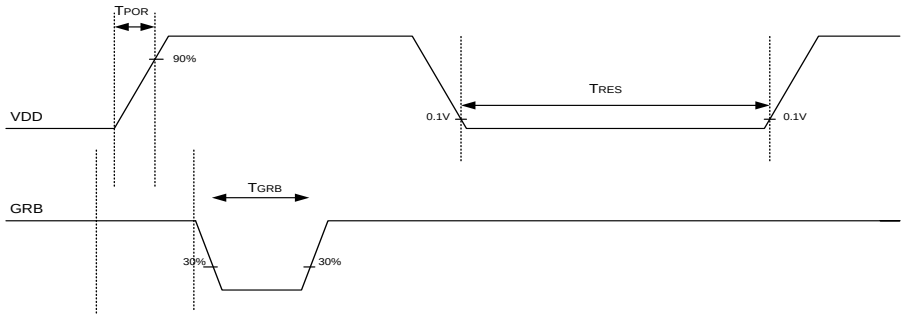
5.4 AC Characteristics

5.4.1 Basic AC Characteristic

(VDD=VDD_IF=1.8V, AVDD=8 to 13.5V, GND=AGND=GND_IF=0V,TA=-20 to +85℃)

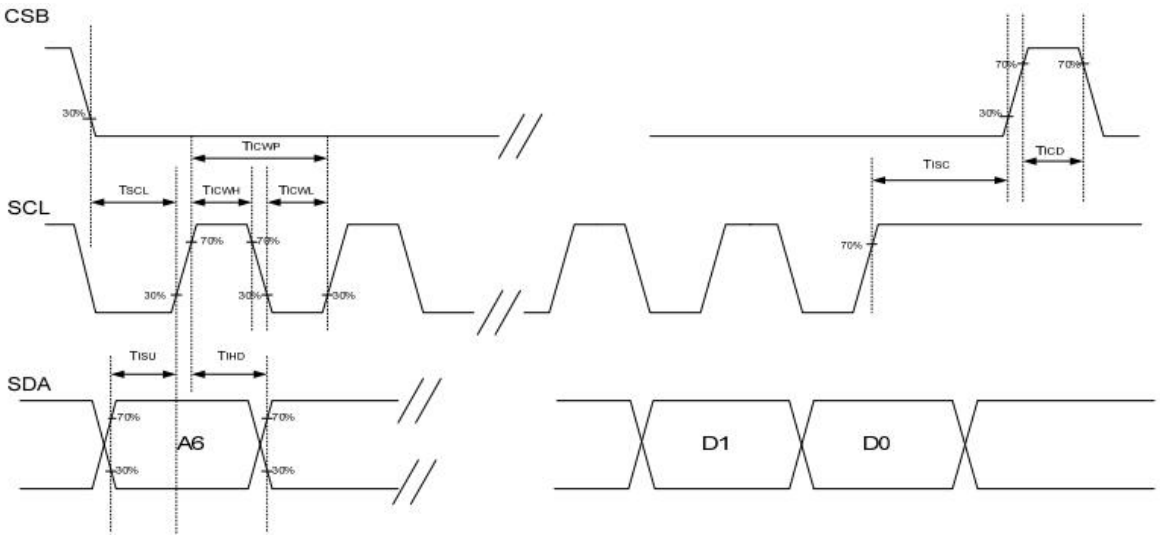
VDD/GRB AC characteristic

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
VDD power slew rate	TPOR	—	—	-20	ms	From 0 to 90% VDD
GRB active pulse width	TGRB	1	—	—	ms	VDD=VDD_IF=1.8V
VDD resettle time	TRES	1	—	—	s	



3-wire interface AC characteristic:

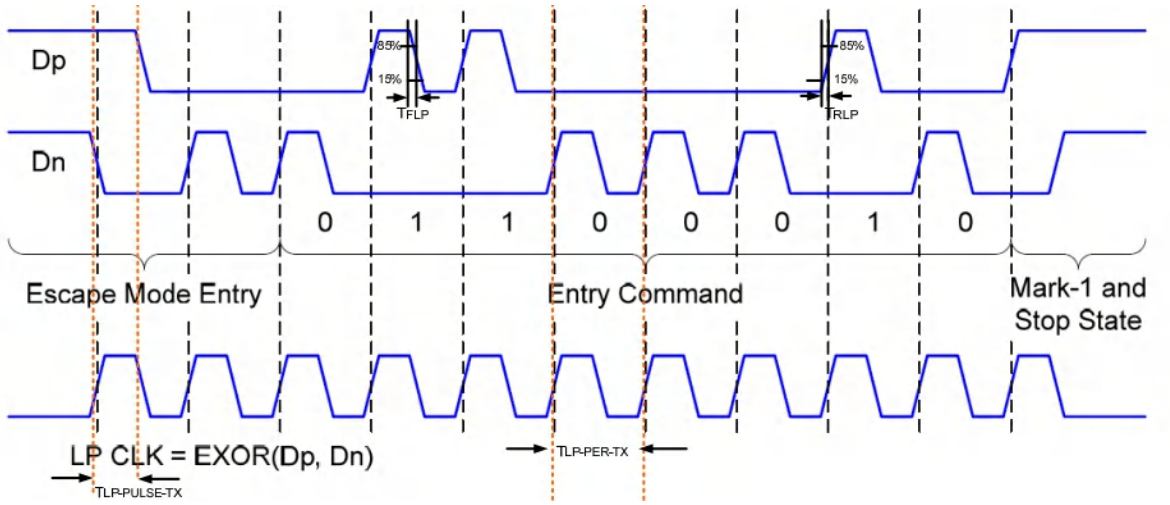
Parameter	Symbol	Min.	Typ.	Max.	Unit
CSB falling to SCL rising	T_{SCL}	200	-	-	ns
SCL pulse high period	T_{ICWH}	100	-	-	ns
SCL pulse low period	T_{ICWL}	100	-	-	ns
SCL pulse width	T_{ICWP}	250	-	-	ns
SDA data input setup time	T_{ISU}	100	-	-	ns
SDA data input hold time	T_{IHD}	100	-	-	ns
SCL to CSB rising time	T_{ISC}	250	-	-	ns
CSB rising to failing time	T_{ICD}	1	-	-	us



5.4.2 MIPI AC Characteristic

- **LP Transmitter AC Specification**

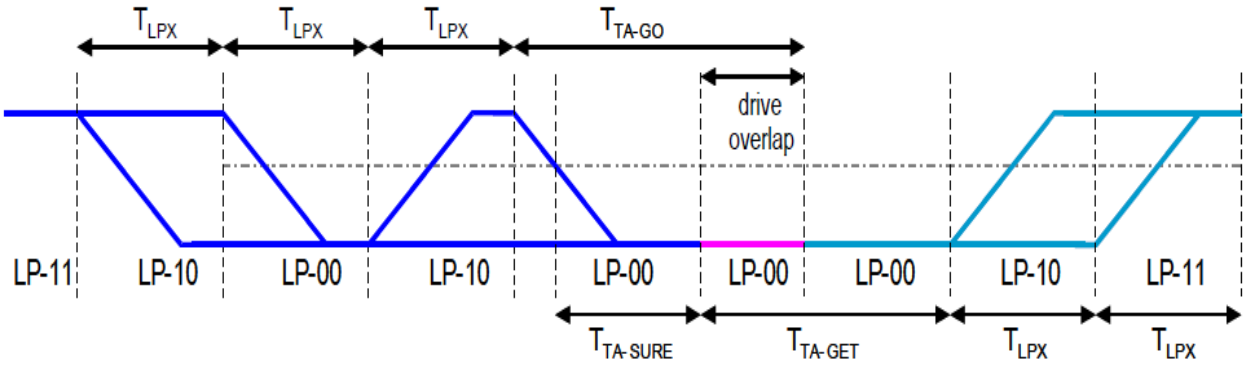
Parameter		Symbol	Min	Typ	Max	Units	Notes
15%~85% rising time and falling time		T_{RLP} /T_{FLP}	-	-	25	ns	-
30%~85% rising time and falling time		T_{REOT}	-	-	35	ns	-
Pulse width of LP exclusive-OR	First LP EXOR clock pulse after STOP state or Last pulse before stop state	$T_{LP-PULSE-TX}$	40	-	-	ns	-
	All other pulses		20	-	-	ns	-
Period of the LP EXOR clock		$T_{LP-PER-TX}$	90	-	-	mV/ns	-
Slew Rate @CLOAD =0pF		$\delta V/\delta t_{SR}$	30	-	500	mV/ns	-
Slew Rate @CLOAD =5pF			30	-	200	mV/ns	-
Slew Rate @CLOAD =20pF			30	-	150	mV/ns	-
Slew Rate @CLOAD =70pF			30	-	100	mV/ns	-
Load Capacitance		T_{RLP}	-	-	70	pF	-



- **Turnaround Procedure**

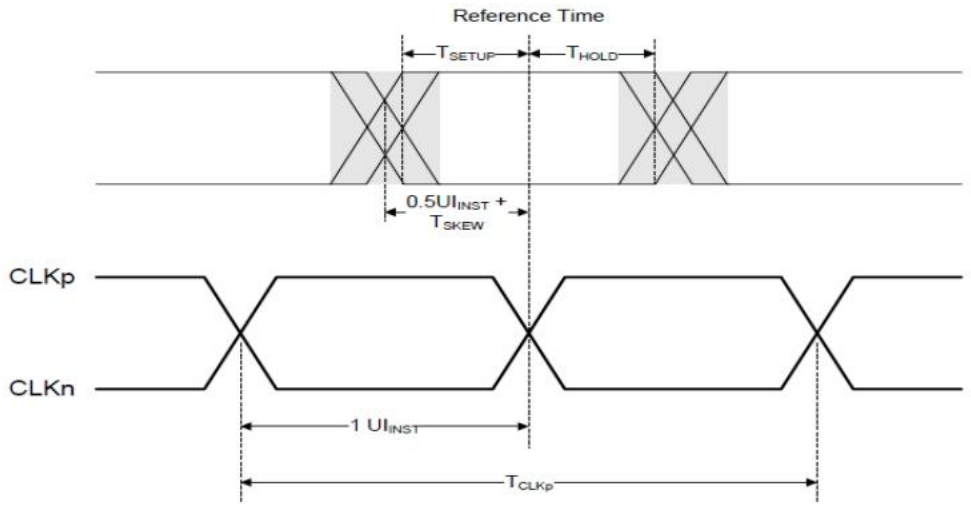
Turnaround Procedure Operation Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
Length of any Low-Power state period: Master side	T_{LPX}	50	-	75	ns
Length of any Low-Power state period: Slave side	T_{LPX}	50	55.56	58.34	ns
Ratio of T_{LPX}(Master)/ T_{LPX} (Slave) between Master and Slave side	Ratio T_{LPX}	2/3	-	3/2	
Time-out before new TX side start driving	$T_{TA-Sure}$	T_{LPX}	-	$2T_{LPX}$	ns
Time to drive LP-00 by new TX	T_{TA-GET}	-	$5T_{LPX}$	-	ns
Time to drive LP-00 after Turnaround Request	T_{TA-GO}	-	$4T_{LPX}$	-	ns



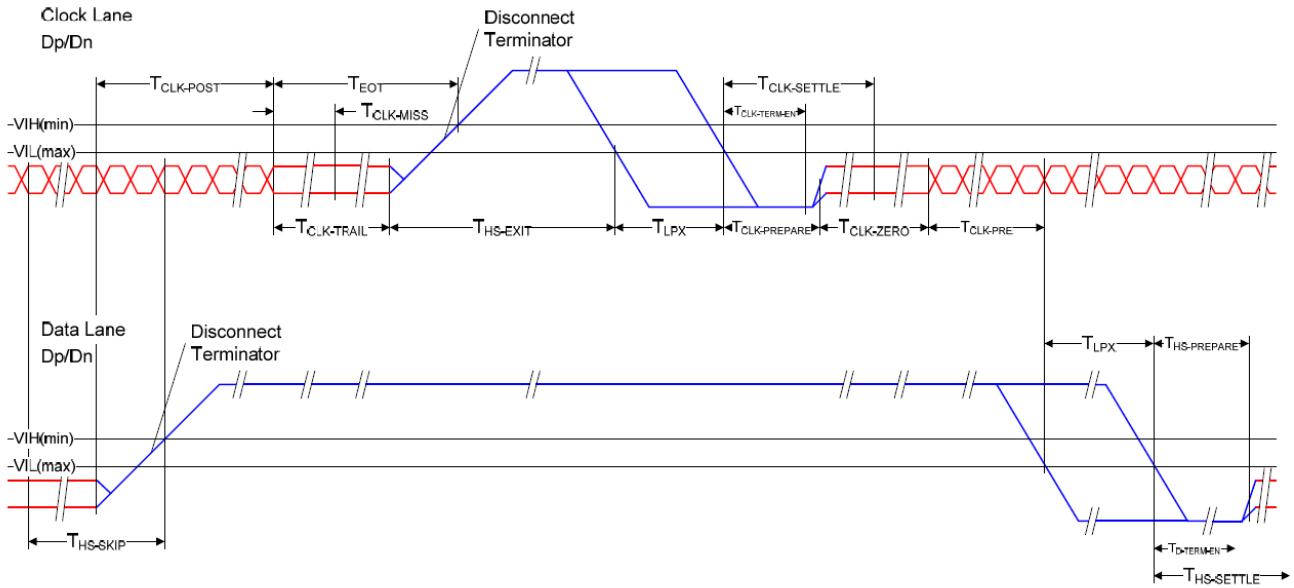
- **High Speed Transmission**

Parameter	Symbol	Min	Typ	Max	Units
UI instantaneous	UI_{INST}	2	-	12.5	ns
Data to Clock Skew(measured at transmitter)	$T_{SKEW(TX)}$	-0.15	-	0.15	UI_{INST}
Data to Clock Setup time(measured at receiver)	$T_{SETUP(RX)}$	0.15	-	-	UI_{INST}
Data to Clock Hold time(measured at receiver)	$T_{HOLD(RX)}$	0.15	-	-	UI_{INST}
20%~80% rise time and fall time	TR, TF	150	-	-	ps
		-	-	0.3	UI_{INST}



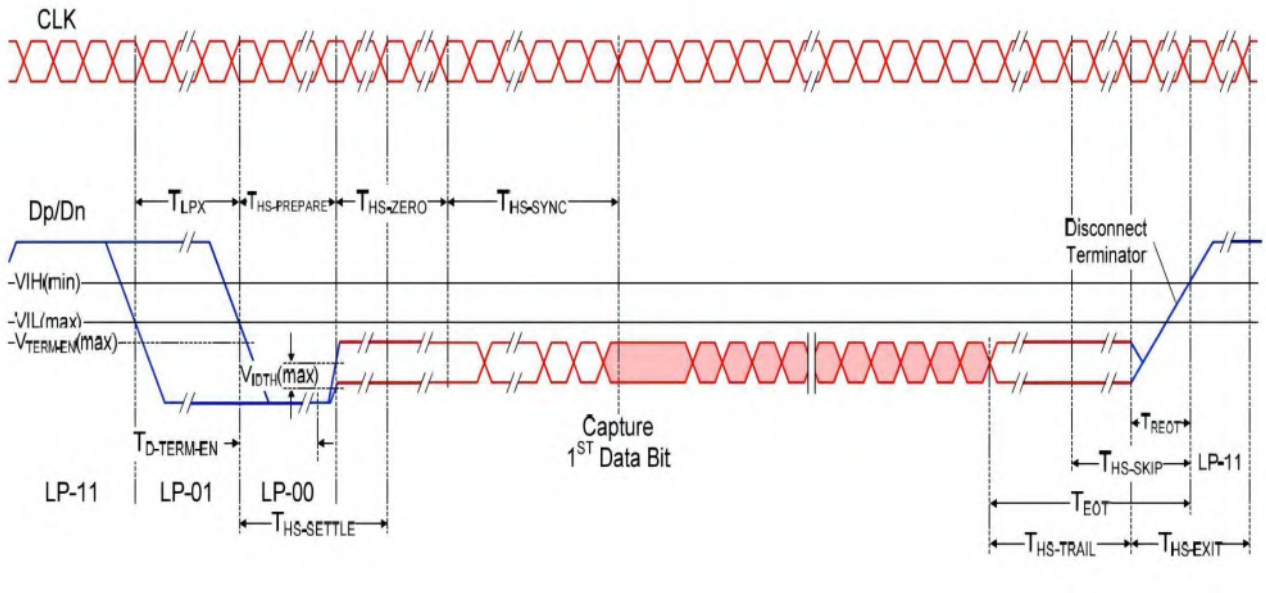
- **High Speed Clock Transmission**

Parameter	Symbol	Min	Typ	Max	Units
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	TCLK-POST	60+52UI	-	-	ns
Detection time that the clock has stopped toggling	TCLK-MISS	-	-	60	ns
Time to drive LP-00 to prepare for HS clock transmission	TCLK-PREPARE	38	-	95	ns
Minimum lead HS-0 drive period before starting clock	TCLK-PREPARE + TCLK-ZERO	300		-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	THS-TERM-EN	-		38	ns
Minimum time that the HS clock must be prior to any associated data lane beginning the transmission from LP to HS mode	TCLK-PRE	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	TCLK-TRAIL	60	-	-	ns



- **Bursts Mode Data Transmission**

Parameter	Symbol	Min	Typ	Max	Units
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of $t_{HS-TRAIL}$ or $t_{CLK-TRAIL}$ period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross $V_{IL,MAX}$	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40	-	55+4UI	ns
Time to drive LP-11 after HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns



Analog Stand-by current	Ist2	No load, clock and all functions are stopped	-	10	50	μA
Input level of V1 ~ V7	Vref1	Gamma correction voltage input	0.4*AVDD	-	AVDD-	V
Input level of V8 ~ V14	Vref2	Gamma correction voltage input	0.1	-	0.6*AVD	V
Output Voltage deviation	Vod1	Vo = AGND+0.1V ~AGND+0.5V and Vo = AVDD-0.5V ~ AVDD-0.1V	-	±20	±35	mV
Output Voltage deviation	Vod2	Vo = AGND+0.5V ~ AVDD-0.5V	-	±15	±20	mV
Output Voltage Offset between Chips	Voc	Vo = AGND+0.5V ~ AVDD-0.5V	-	-	±20	mV
Dynamic Range of Output	Vdr	SO1 ~ 1536	0.1	-	AVDD-0.1	V
Sinking Current of Outputs	IOLy	SO1 ~ 1536; Vo=0.1V v.s 1.0V , AVDD=13.5V	80	-	-	uA
Driving Current of Outputs	IOHy	SO1 ~ 1536; Vo=13.4V v.s12.5V , AVDD=13.5V	80	-	-	uA
Resistance of Gamma Table	Rg	Rn: Internal gamma resistor	0.7*Rn	1.0*Rn	1.3*Rn	ohm

(VDD=VDD_IF=1.8V,AVDD=8 to 13.5V,GND=AGND=GND_IF=0V,TA=-20℃ to 85℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
MIPI Characteristics for High Speed Receiver					
Single-ended input low voltage(DSI-CLKP/N,DSI-DnP/N)	VILHS	-40	—	—	mV
Single-ended input high voltage (DSI-CLKP/N,DSI-DnP/N)	VIHHS	—	—	460	mV
Input Common-mode voltage (DSI-CLKP/N,DSI-DnP/N)	VCDRXDC	70	—	330	mV
Differential input impedance	ZID		100		ohm
HS transmit differential voltage(VOD=VDP-VDN)	|VOD|	140	200	250	mV
Low-level differential input voltage threshold	VTHLCLK VTHLDATA	-70	—	—	mV
High-level differential input voltage threshold	VTHHCLK VTHHDATA	—	—	—	mV
Single-ended threshold voltage for termination	VTERN_EN	—	—	450	mV
Termination capacitor	CTERM		—	14	pf
Input voltage common mode variation(<=450Mhz)	VCMRCLK VCMRDATAL	-50	—	50	mV
Input voltage common mode variation(>=450Mhz)	VCMRCLKM VCMRDATAM	—	—	100	mV
MIPI Characteristics for Low Power Mode					
Pad signal voltage range	VI	-50	—	1350	mV
Ground shift	VGNDSH	-50	—	50	mV
Logic 0 input threshold	VIL	0	—	550	mV
Logic 1 input threshold	VIH	880	—	1350	mV
Logic 0 input voltage LPRX(CLK,ULP mode)	VILLPRXULP	0	—	300	mV
Input hysteresis	VHYST	25	—	—	mV
Output low level	VOL	-50	—	50	mV
Output high level	VOH	1.1	1.2	1.3	V
Output impedance of Low Power Transmitter	ZOLP	90	100	110	ohm

5.4.3 Input Timing for MIPI

HV mode
Vertical input timing

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Vertical display area	tvd		600		H
VSYNC period time	tv	624	635	750	H
VSYNC pulse width	tvpw	1	10	20	H
VSYNC back porch	tvb	23	23	23	H
VSYNC front porch	tvfp	1	12	127	H

HV mode
Horizontal input timing

Parameter		Symbol	Value			Unit
Horizontal display area		thd		1024		DCLK
DCLK frequency@ Frame rate=60hz		fclk	Min.	Typ.	Max.	
			44.9	51.2	63	Mhz
1 Horizontal Line		th	1200	1344	1400	DCLK
HSYNC pulse width	Min.	thpw		1		
	Typ.			70		
	Max.			140		
HSYNC blanking		thb	160	160	160	
HSYNC front porch		thfp	16	160	216	

6.0 OPTICAL CHARACTERISTICS

3.1 Optical Specifications

Item	Symbol	Temp	Condition	Min	Typ	Max	Unit	Remark
Viewing Angle range	Horizontal	θ	CR > 10	80	85	--	Deg	Note 1
	Vertical	θ		80	85	--	Deg	
Luminance Contrast ratio		CR	θ = 0°	600：1	800	--	--	Note 2
Brightness		YL		800	1000	--	Cd/cm2	
Transmittance		T(%)	θ = 0°		5.0		%	Note 3
Color Gamut (C light)				--	50	--	%	
White chromaticity		Wx	Θ=0°	TYP. -0.03	0.306	TYP. +0.03		Note 4
		Wy			0.336			
Reproduction of color （C-light）	Red	Rx			0.599			
		Ry			0.338			
	Green	Gx			0.299			
		Gy			0.550			
	Blue	Bx			0.139			
		By			0.131			
Response Time (Rising + Falling)	Trt		Ta= 25°C θ = 0°	--	30	40	ms	Note 5

3.2 Measuring Condition

Measuring surrounding: dark room ,LED current IL : 360mA
Ambient temperature: 25±2℃ 15min. warm-up time.

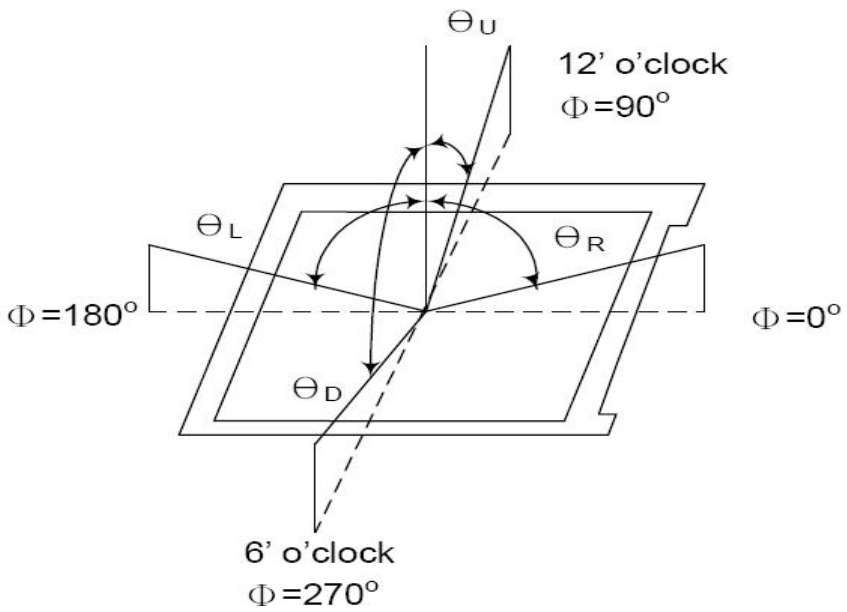
3.3 Measuring Equipment

7.0 Reliability test items

Test Item	Test Conditions	Notes
High temperature Operation	Ta= +70℃, 120hrs	
Low temperature Operation	Ta= -20℃, 120hrs	
High Temperature Storage	Ta= +80℃, 120hrs	
Low Temperature Storage	Ta= -30℃, 120hrs	
Humidity Test	60℃ ,Humidity 90% ,96hrs	
Thermal Shock Test	-20℃,30min ~ +60℃,30min (30 cycle)	
Vibration Test(Packing)	Sine Wave 1.04G, 5~500Hz, XYZ 30min/each direction	

FPM520 of Westar Display technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics. Measuring spot size: 20 ~ 21 mm

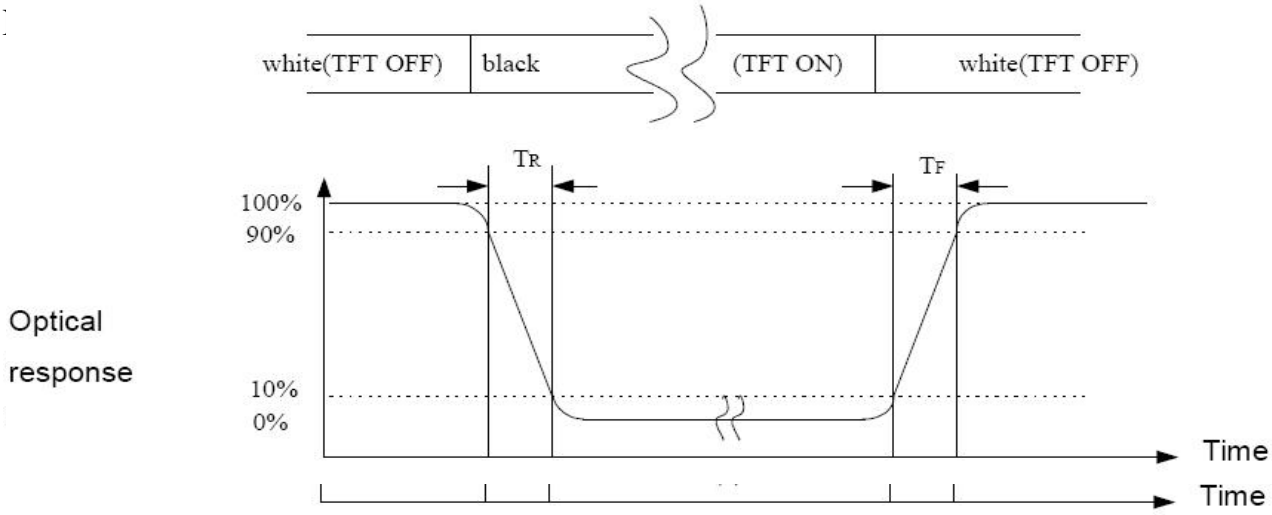
Note (1) Definition of Viewing Angle :



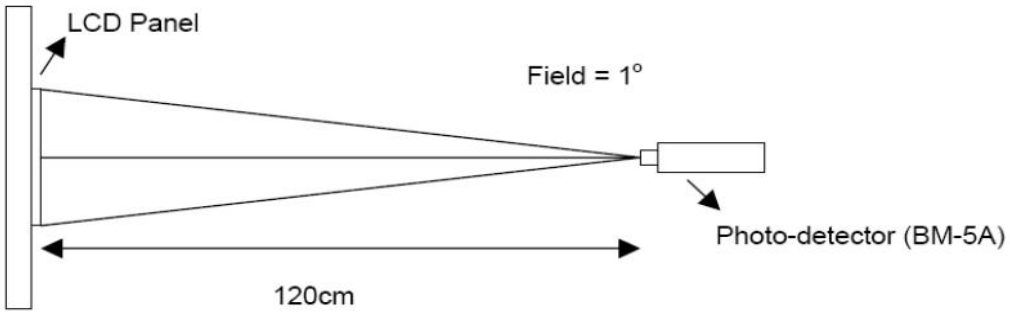
Note (2) Definition of Contrast Ratio (CR):
Measured at the center point of panel

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

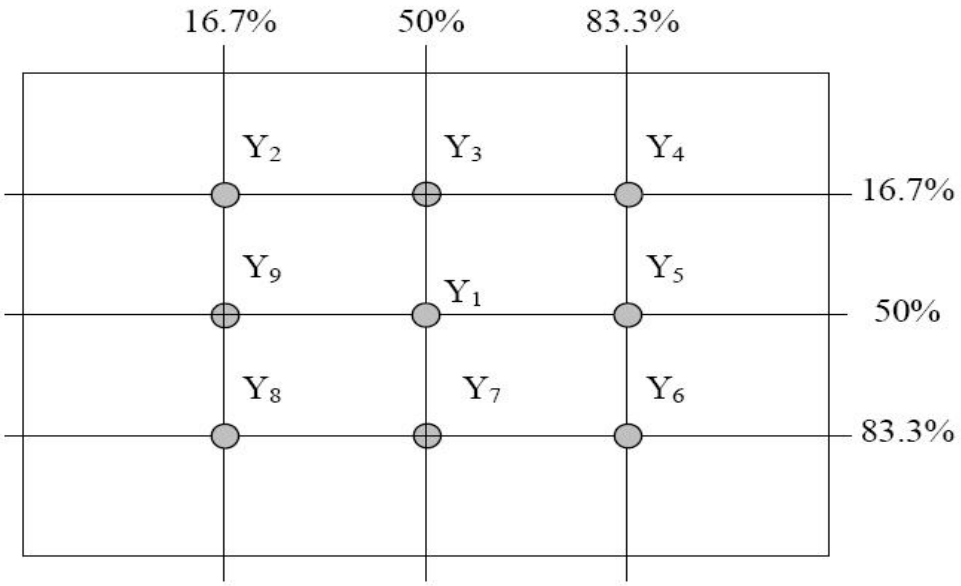
Note (3) Definition of Response Time: Sum of TR and TF



Note (4) Definition of optical measurement setup

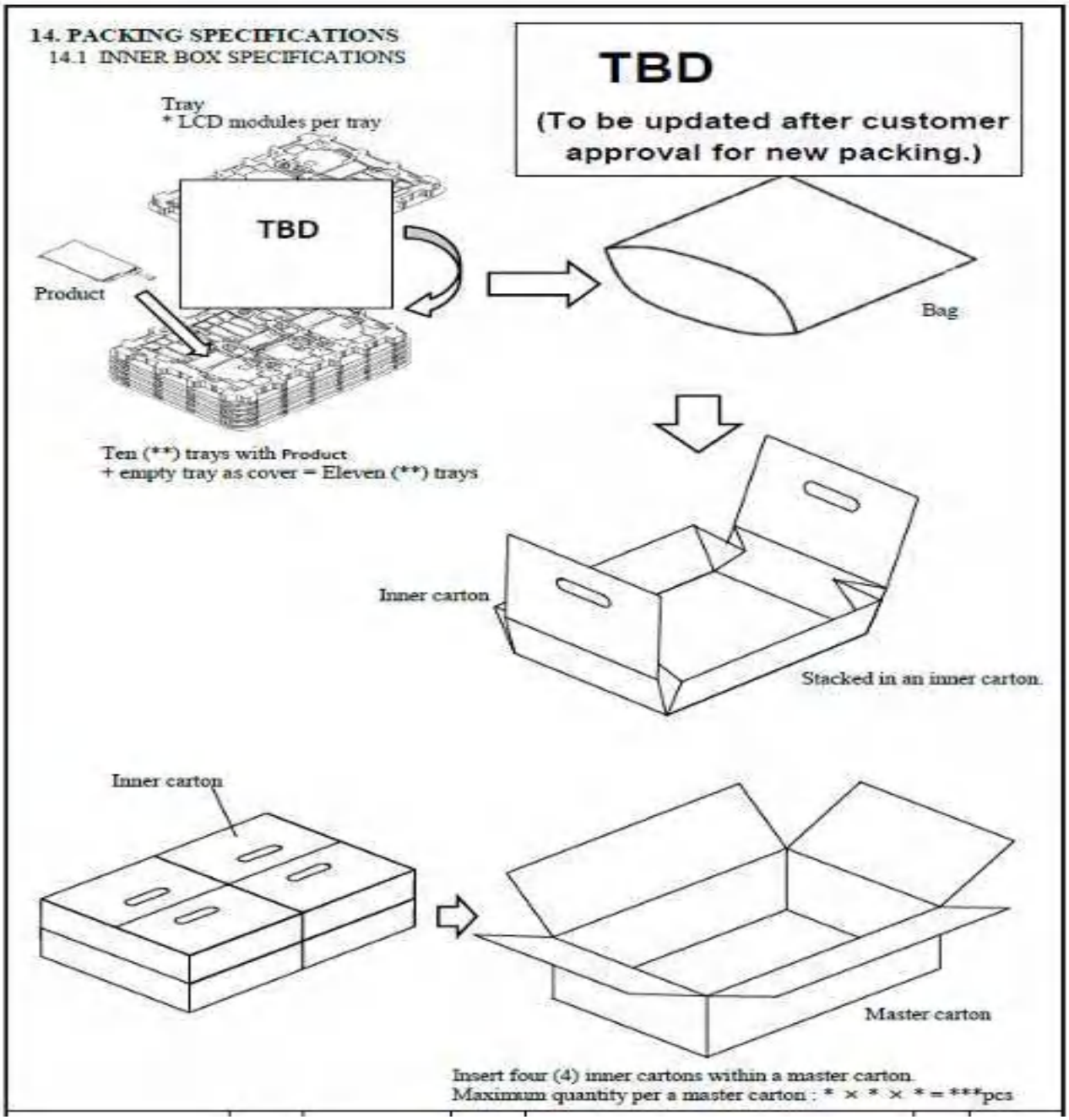


Note (5) Definition of brightness uniformity



$$\text{Luminance uniformity} = \frac{\text{(Min Luminance of 9 points)}}{\text{(Max Luminance of 9 points)}} \times 100\%$$

8.0 Packing


14. PACKING SPECIFICATIONS
14.1 INNER BOX SPECIFICATIONS
TBD
(To be updated after customer approval for new packing.)
Tray
* LCD modules per tray
TBD
Product
Bag
Ten (**) trays with Product
+ empty tray as cover = Eleven (**) trays
Inner carton
Stacked in an inner carton.
Inner carton
Master carton
Insert four (4) inner cartons within a master carton.
Maximum quantity per a master carton : * × * × * = ***pcs

9.0 General precaution

9.1 Use Restriction

This product is not authorized for use in life supporting systems, aircraft navigation control systems, military systems and any other application where performance failure could be life threatening or otherwise catastrophic.

9.2 Disassembling or Modification

Do not disassemble or modify the module. It may damage sensitive parts inside LCD module, and may cause scratches or dust on the display. HT does not warrant the module, if customers disassemble or modify the module.

9.3 Breakage of LCD Panel

9.3.1.If LCD panel is broken and liquid crystal spills out, do not ingest or inhale liquid crystal, and do not contact liquid crystal with skin.

9.3.2. If liquid crystal contacts mouth or eyes, rinse out with water immediately.

9.3.3. If liquid crystal contacts skin or cloths, wash it off immediately with alcohol and rinse thoroughly with water.

9.3.4. Handle carefully with chips of glass that may cause injury, when the glass is broken.

9.4 Electric Shock

9.4.1. Disconnect power supply before handling LCD module.

9.4.2. Do not pull or fold the LED cable.

9.4.3. Do not touch the parts inside LCD modules and the fluorescent LED's connector or cables in order to prevent electric shock.

9.5 Absolute Maximum Ratings and Power Protection Circuit

9.5.1. Do not exceed the absolute maximum rating values, such as the supply voltage variation, input voltage variation, variation in parts' parameters, environmental temperature, etc., otherwise LCD module may be damaged.

8.5.2. Please do not leave LCD module in the environment of high humidity and high temperature for a long time.

8.5.3. It's recommended to employ protection circuit for power supply.

9.6 Operation

9.6.1 Do not touch, push or rub the polarizer with anything harder than HB pencil lead.

9.6.2 Use finger stalls of soft gloves in order to keep clean display quality, when persons handle the LCD module for incoming inspection or assembly.

9.6.3 When the surface is dusty, please wipe gently with absorbent cotton or other soft material.

9.6.4 Wipe off saliva or water drops as soon as possible. If saliva or water drops contact with polarizer for a long time, they may causes deformation or color fading.

9.6.5 When cleaning the adhesives, please use absorbent cotton wetted with a little petroleum benzine or other adequate solvent.

9.7 Mechanism

Please mount LCD module by using mouting holes arranged in four corners tightly.

9.8 Static Electricity

9.8.1 Protection film must remove very slowly from the surface of LCD module to prevent from electrostatic occurrence.

9.8.2. Because LCD module use CMOS-IC on circuit board and TFT-LCD panel, it is very weak to electrostatic discharge. Please be careful with electrostatic discharge. Persons who handle the module should be grounded through adequate methods.

9.9 Strong Light Exposure

The module shall not be exposed under strong light such as direct sunlight. Otherwise, display characteristics may be changed.

9.10 Disposal

When disposing LCD module, obey the local environmental regulations.